THE UNIVERSITY OF ALBERTA

A HIGH SPEED ANALOG-TO-DIGITAL ENCODER

by

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The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies for acceptance, a thesis entitled "A High Speed Analog-to-Digital Encoder" submitted by Donald F. McFarlane in partial fulfillment of the requirements for the degree of Master of Science.

ABSTRACT

This thesis deals with the design and construction of an encoder which converts an analog voltage to its digital representation.

The input voltage is sampled, quantized in ten-millivolt steps and encoded, giving an eleven bit parallel digital output in binary code. The encoder has a range of plus and minus ten volts and a constant conversion time of twenty microseconds, enabling operation up to 50,000 conversions per second, the rate being determined by an external trigger pulse source.

The encoder is to be used with a magnetic core memory and a digital-to-analog converter to provide a time delay, which is necessary in many analog computer simulations.

ACKNOWLEDGEMENTS

The writer wishes to express his appreciation for assistance received during the preparation of this work. The research described in this thesis was carried out at the University of Alberta under the supervision of Professor Y.J. Kingma, to whom the writer wishes to acknowledge his indebtedness for advice and assistance throughout the project.

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INTRODUCTION

1.1. Simulation of Time Delays

One of the difficult problems encountered in analog computation is the simulation of a pure time delay, a situation which occurs in the study of many physical systems. In the frequency domain, a time delay has the following property: When a complex signal is subjected to a time delay, each of its frequency components is unchanged in amplitude but undergoes a phase shift directly proportional to its frequency. Most of the solutions to the problems of simulating a time delay have serious limitations as to accuracy, stability, frequency response and flexibility.

Digital techniques provide a very satisfactory method of simulating a time delay. The analog input voltage to be delayed is sampled at a rate greater than twice its highest frequency component. Each sample is converted to digital form and stored in a memory for the required delay time. It is then recovered from the memory and converted back to an analog voltage. There are two principal sources of

Chapter 1

Introduction

1.1. Motivation: Is time delay

One of the defining problems encountered in analog communication is the distortion of a pure time delay, a problem which occurs in its plain or filtered guises. In the frequency domain, a time delay is the relative incoherency that arises between a signal and its time-delayed counterpart as manifested in destructive and constructive interference. Some of this behavior is the problem of cancelling a time delay into another dimension or to accelerate quantity through frequency regions and (possibly-

digital luminaries provide a very seductive and method of simulating a time delay. One simple idea suggests it be delayed is sampled in a bucket brigade time delay (a digital flow was sampled in a memory for this temporal delay time. It is then recovered from the memory and summed back in at some volume. There are two potential sources of

error in a digital time delay, the finite sampling rate and the quantization of the input voltage. Errors resulting from the finite sampling rate are a phase shift proportional to frequency and a loss in amplitude roughly proportional to frequency; these errors are small, however, if the sampling rate is much greater than the highest frequency component of the signal being delayed. The quantization error is caused by the approximation of the analog voltage by one of a number of fixed voltage levels, a necessary part of analog-to-digital conversion. This error can be kept small if the separation between the fixed voltage levels is small compared to the magnitude of the input voltage range. The use of many small voltage increments also minimizes the amplification of noise when the analog voltage lies between two adjacent voltage levels, although the output noise caused by the encoder switching between one level and the next cannot easily be eliminated. A digital time delay has the additional advantage of flexibility, in that the delay time can be very easily adjusted over a wide range with no adverse effect on accuracy (subject to the above limitation on sampling rate).

The subject of this thesis is the design and construction of an analog-to-digital encoder which is

to be used as a part of a digital time delay. Details of the accompanying magnetic core memory unit and the digital-to-analog decoder are given in Ref. 1 and 2. The encoder also has a potential application as a link between an analog and a digital computer, making possible the simulation of problems by using hybrid computation techniques, and in the preparation of experimental data for digital computer analysis.

1.2. Statement of Problem

To design an analog-to-digital converter with the following specifications:

1) a conversion rate adjustable from zero to 50,000 conversions per second.
2) one thousand quantized steps plus a sign bit.
3) two input voltage ranges, $\pm$ 10 volts and $\pm$ 100 volts.
4) binary code to be used, with the digital output in parallel form and held for at least two microseconds.
5) output logic: 0 -- 0 volts
   1 -- -5 volts
6) sign bit: 0 -- positive input voltage
   1 -- negative input voltage
7) a sample-hold circuit to be included.
8) drift over a 10° C. temperature range to be less than one quantized step.

1.3. Analog-to-Digital Encoders

In the literature many methods for accomplishing analog-to-digital conversion are described; the most important of these methods, and their suitability for meeting the specifications for this project, are discussed here.

The most elementary method of conversion is the simultaneous method, in which the input voltage is compared directly to a number of reference voltages. This is the fastest method of conversion, but in general to obtain a resolution of N bits, 2^{N-1} comparators are required. For resolution greater than three or four bits the numbers of comparators and reference voltages necessary and the complexity of the logic required become prohibitive.

The method of successive comparisons described by Smith (Ref. 3) can be conveniently applied on an analog computer, where all the required components are available. A number of stages (like that shown in Fig. 1), equal to the desired number of binary digits, is required. V_r is a reference voltage equal to half the maximum expected input voltage, and is the same for each stage. If V_{in} is less than V_r, the binary output is a 0 and the analog output is zero volts.

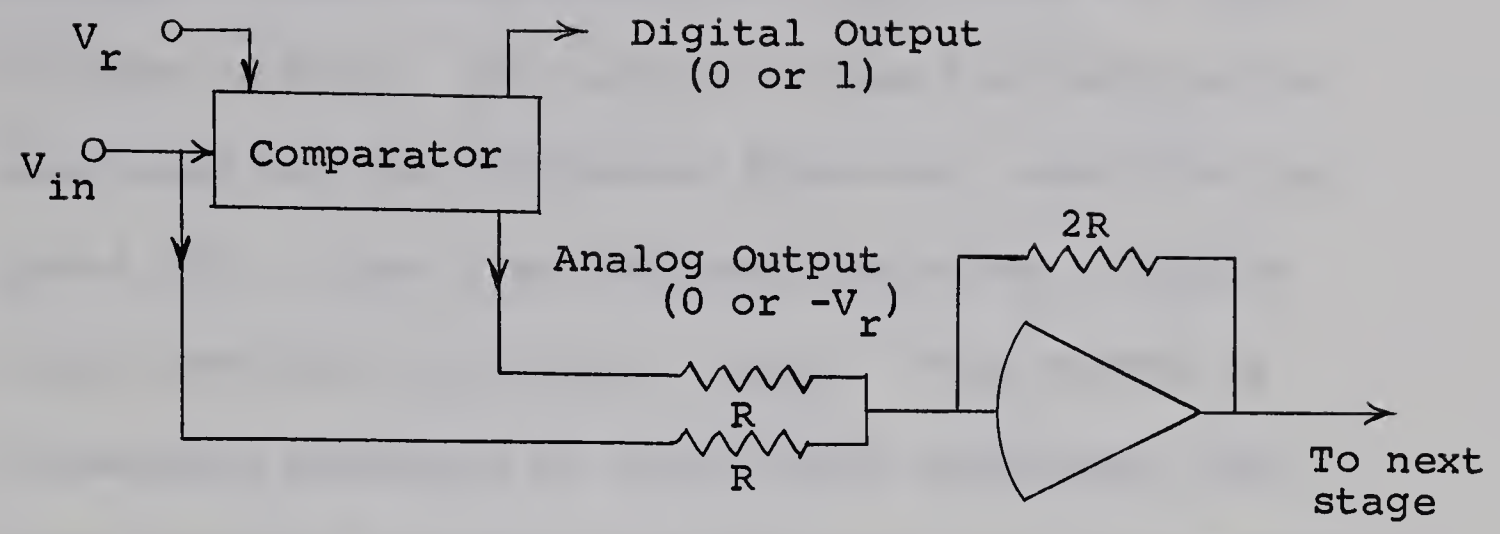


Figure 1. Successive Comparison Encoder

V_{in} is then doubled by the operational amplifier and applied to the next stage. If V_{in} is greater than V_r, the binary output is a 1 and the analog output is $-V_r$ volts. Then V_r is subtracted from V_{in}, and the difference is doubled and applied to the next stage.

The major disadvantage of this method is that any error or noise in one stage is doubled in each remaining stage. Thus for an overall accuracy of 0.1%, the allowable error and noise contributed by the first stage would be less than 0.0002%, or 20 microvolts for a ten volt range. Since this requirement is extremely difficult to meet, the method was considered unsuitable.

The frequency modulation method given by Rigby (Ref. 4) utilizes two oscillators, one operating at a constant frequency and the other providing a frequency which is a linear function of the input

Comparator

voltage. These frequencies are equal when the input voltage is zero. The outputs of the two oscillators are mixed and the difference frequency, amplified and gated for a fixed time interval, actuates a counter which provides the digital output. This method of conversion possesses no significant advantages over other methods in speed or simplicity, and the requirement for a voltage-controlled oscillator with a sufficiently linear relationship between voltage and frequency is difficult to meet at high frequencies.

The feedback or successive approximation converter shown in Fig. 2 is a common approach to analog-to-digital conversion, used in several commercial encoders. The register consists of a series of flip-flops which serves as a memory during each conversion. Initially all the flip-flops in the register are set to the zero state. When the encoding process begins, the control unit sets the first flip-flop in the register (which represents the most significant bit) to the one state. This produces an output voltage from the digital-to-analog decoder of half the full-scale voltage. If the input voltage is less than this, the comparator signal causes the control unit to reset that flip-

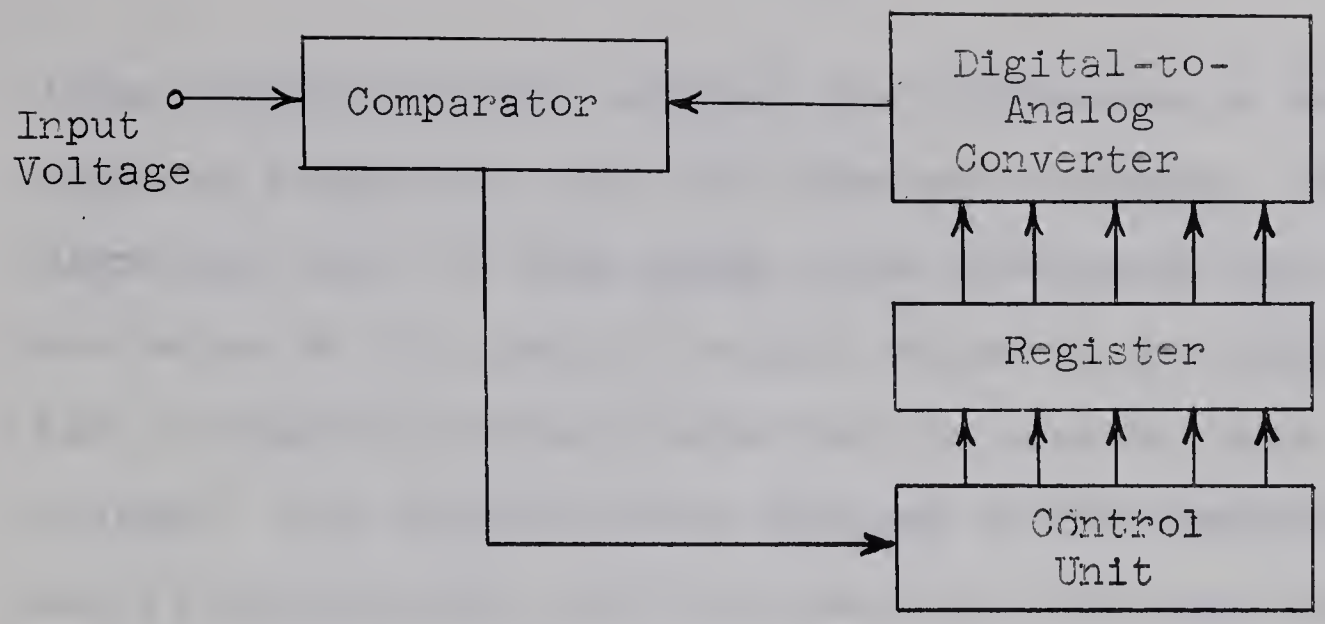
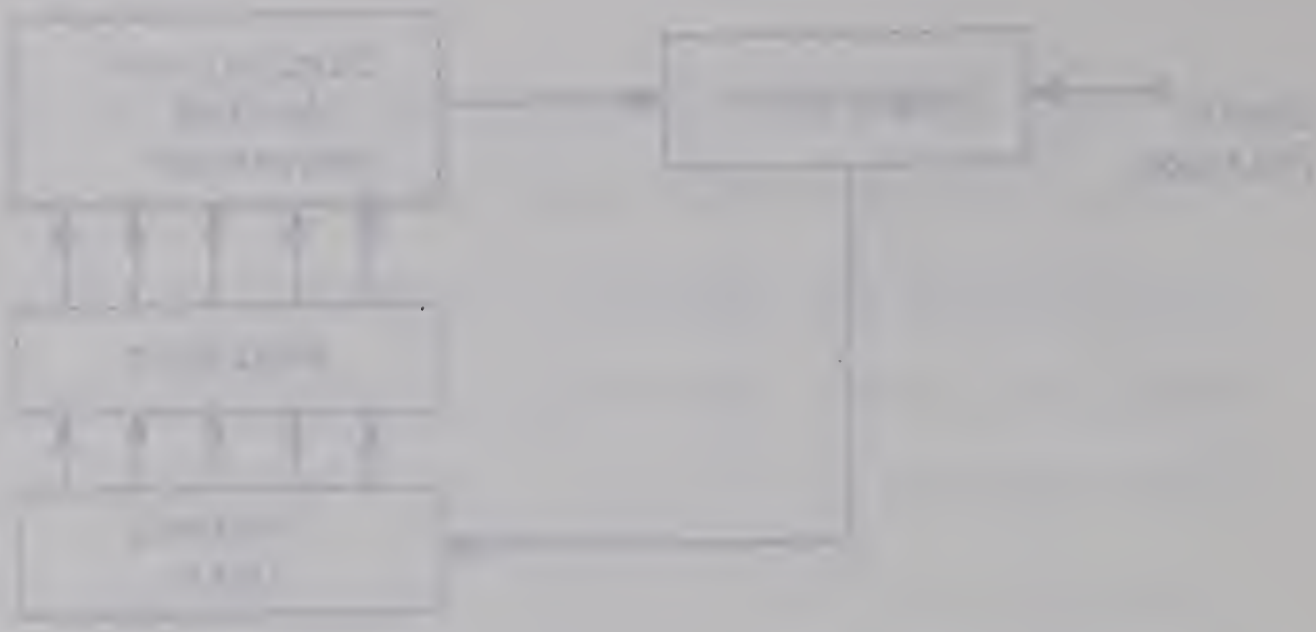


Figure 2. Successive Approximation Encoder

flop to the zero state; if the input voltage is greater than the decoder voltage, the flip-flop is left in the one state. This process is repeated with each flip-flop in the register. At the end of the conversion the decoder output is equal to the input voltage (within the quantization error) and the digital output may be taken from the register. The necessity of constructing a digital-to-analog decoder having an accuracy at least as great as the desired encoder accuracy is the major drawback of this method.

Feyrer (Ref. 5) designed an encoder based upon a modification of the above method, in which the register is not reset between conversions. At the beginning of each conversion the value of the previous sample is stored in the register and is available as an analog voltage from the decoder. This voltage is subtracted from the input voltage to obtain the change in



input voltage between samples; the difference is encoded by comparison with six reference voltages. The digitized error is then added to or subtracted from the value of the previous sample stored in the register, giving the correct value for the present input voltage. The encoding time obtained in this encoder was 16 microseconds, and the resolution obtained was one part in 64, considerably less than that attempted in this thesis.

The approach used in this thesis is the ramp encoder method, which will be described in detail in Chapter 2. This method was chosen because it seemed adequate for meeting the specifications for this project, and because no recent work on ramp encoders was found in the literature.

References 6, 7, 8 and 9 give more detailed information on several types of encoders, as well as general discussions of analog-to-digital conversion.

CHAPTER 2

THE RAMP ENCODER

2.1. Principles of Operation

The operation of a ramp encoder depends upon the conversion of the analog voltage into a time interval which is proportional to this voltage. The time interval is then measured to obtain a digital representation of the analog voltage.

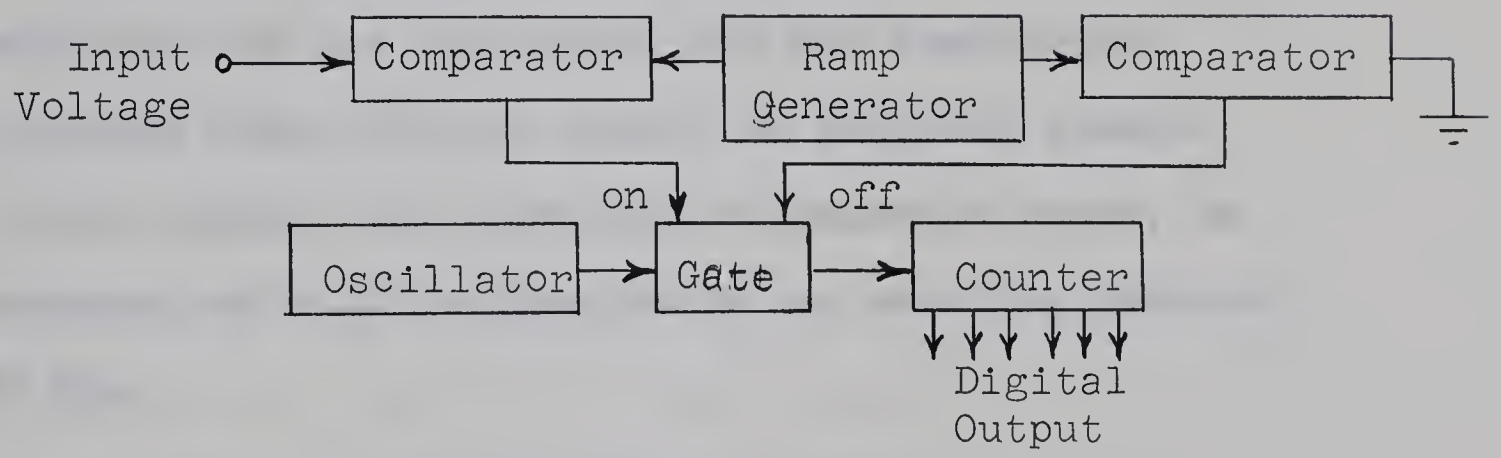


Figure 3. Ramp Encoder

A linear voltage ramp is generated and applied to two comparators, as shown in Fig. 3. One produces a pulse when the ramp voltage is equal to the input voltage, and the other generates a pulse when the ramp crosses zero volts. These two pulses define a time interval which is proportional to the input voltage. They are used to turn on and off a gate which, while conducting, transmits pulses

from an oscillator which are counted by a binary counter composed of a series of flip-flops. After the gate has been turned off, the number held in the counter is the digital representation of the input voltage. When this number has been read out and the counter reset to zero, the encoder is ready for another conversion.

The accuracy of a ramp encoder depends primarily on the linearity of the ramp and on the stability of the oscillator and the comparators. Although these factors cannot be improved indefinitely without the sacrifice of encoding speed, an accuracy of 0.1% is feasible at an encoding rate of 50 khz.

The major difficulty in designing a fast ramp encoder is that, to achieve an accuracy of N binary bits, the oscillator frequency must be higher than the maximum encoding rate by a factor of 2^N. For 50 khz. operation with ten bit accuracy the oscillator frequency must be 51.2 megahertz, or higher if time is allowed for sampling, readout and reset within the 20 microsecond period. This imposes severe restrictions on the switching times of the flip-flops in the counter.

2.2. Circuit Refinements

The simplified encoder of Fig. 3 is unsatisfactory in several respects, and a number of additional circuits are required in order to make a useful encoder. To provide a high and constant input impedance and to isolate the input voltage source from the rest of the encoder, an operational amplifier is used at the input. This also provides for convenient switching between the $\pm$10 volt and $\pm$100 volt ranges, simply by changing the input resistor of the operational amplifier. It also offers a means of overload protection by limiting the summing junction voltage, which prevents damage both to the encoder and to the signal source.

The encoder must be capable of encoding both positive and negative input voltages. One possible method for arranging this is the use of a ramp going from +10 to -10 volts, and the extraction of the polarity information from the order in which the comparator pulses occur. This, however, would require that the oscillator frequency be doubled if the same maximum encoding rate were desired. The oscillator frequency would then be in excess of one hundred megahertz, and the highest speed flip-flop in

the counter would be required to switch with a rise-time of the order of two nanoseconds. With the components available this was found to be impractical.

In order to handle voltages of both polarities an absolute value circuit is used, ensuring that the voltage to be encoded is always of one polarity, and providing the polarity information for the sign bit. One of the most important considerations in the choice of an absolute value circuit is the maximum expected rate of change of the input voltage (as derived in Section 3.1). As the input voltage to a precision absolute value circuit passes through zero, there is always some time delay before the circuit can change state and produce the proper output voltage. This causes an error of the type shown in Fig. 4, the magnitude of which is directly proportional to this time delay T_d and to the rate of change of the input voltage.

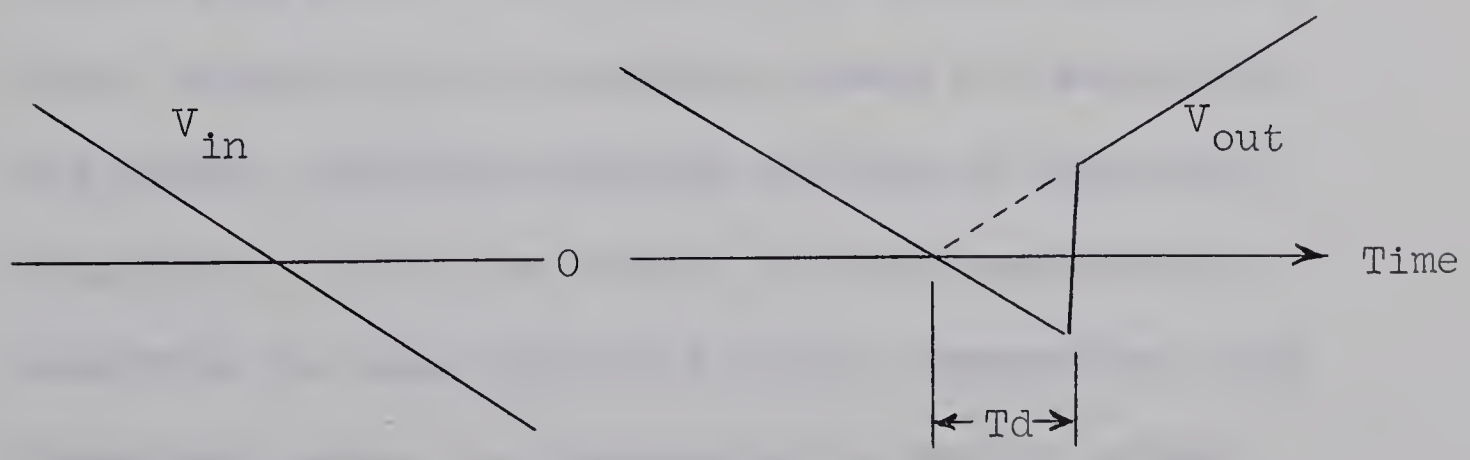
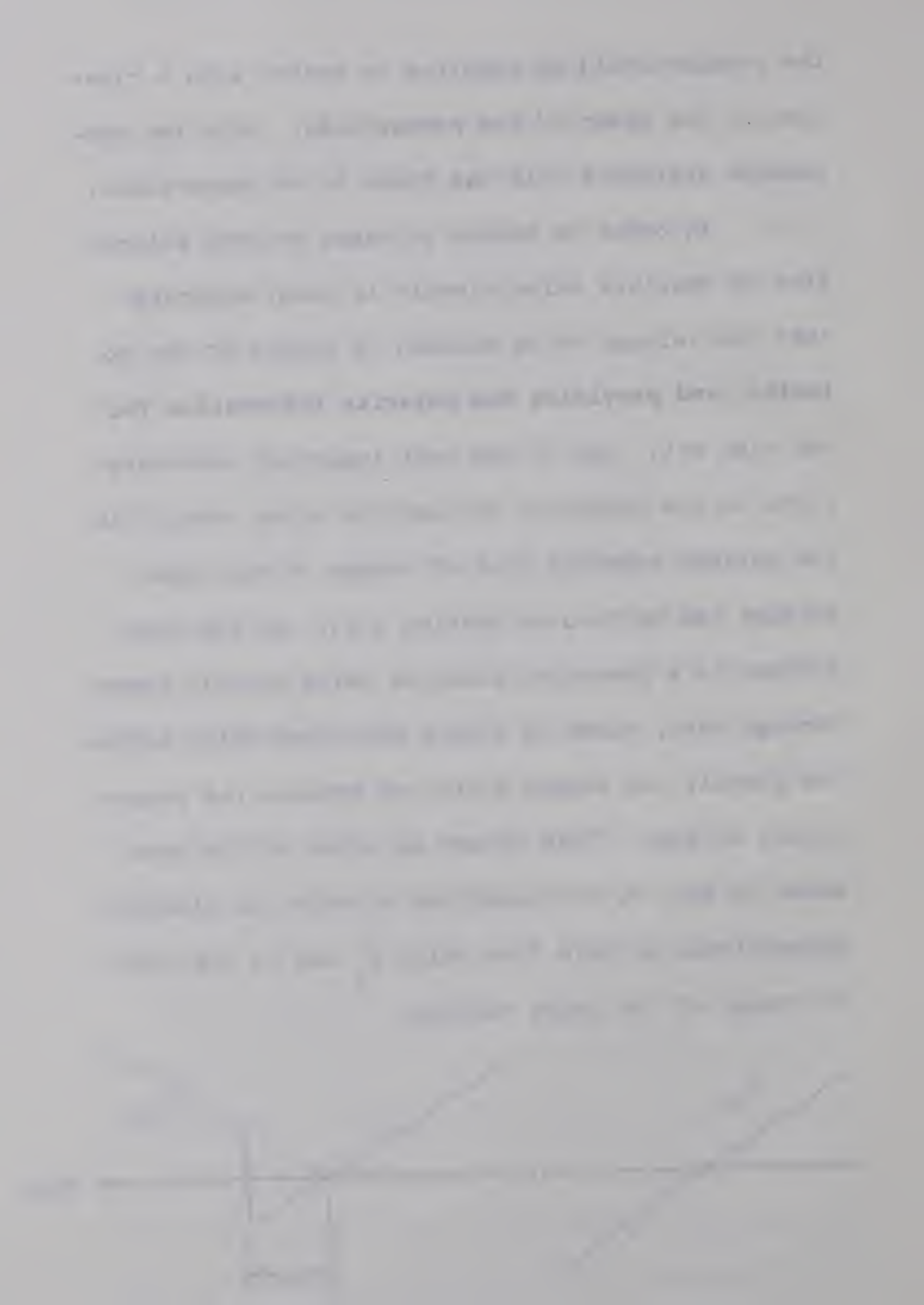
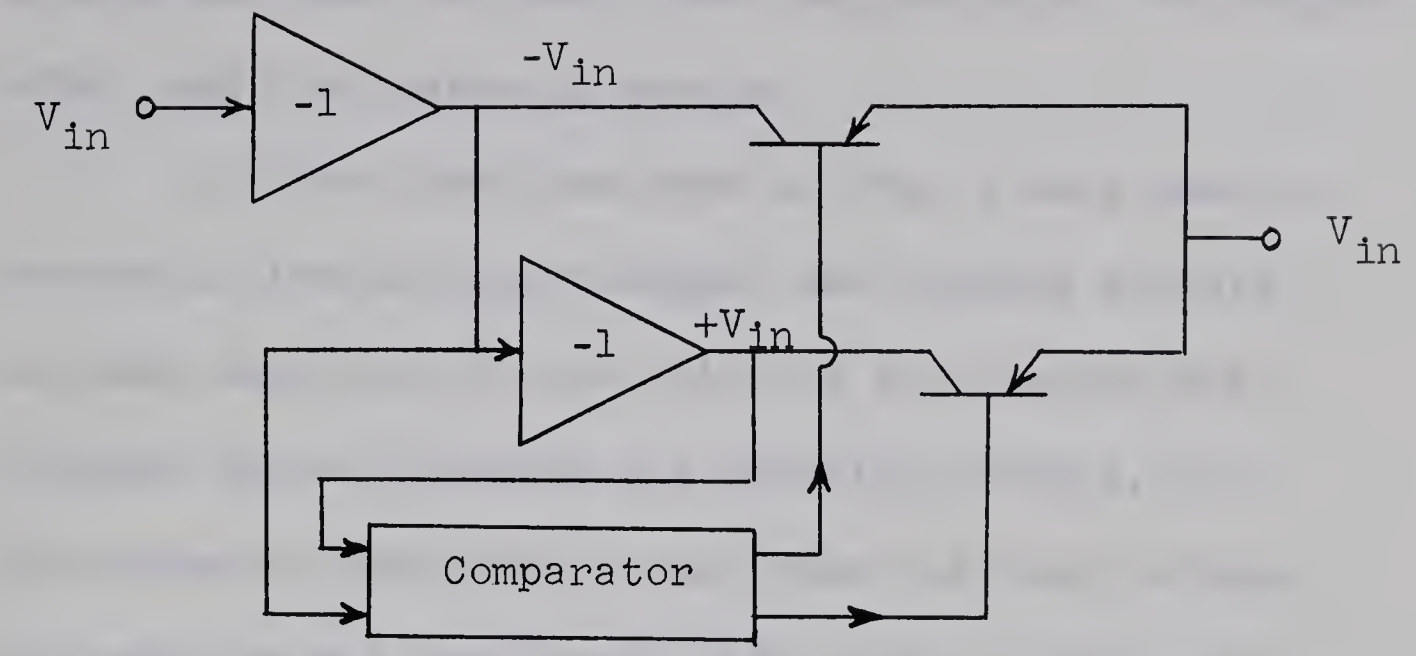


Figure 4. Error in Absolute Value Circuit

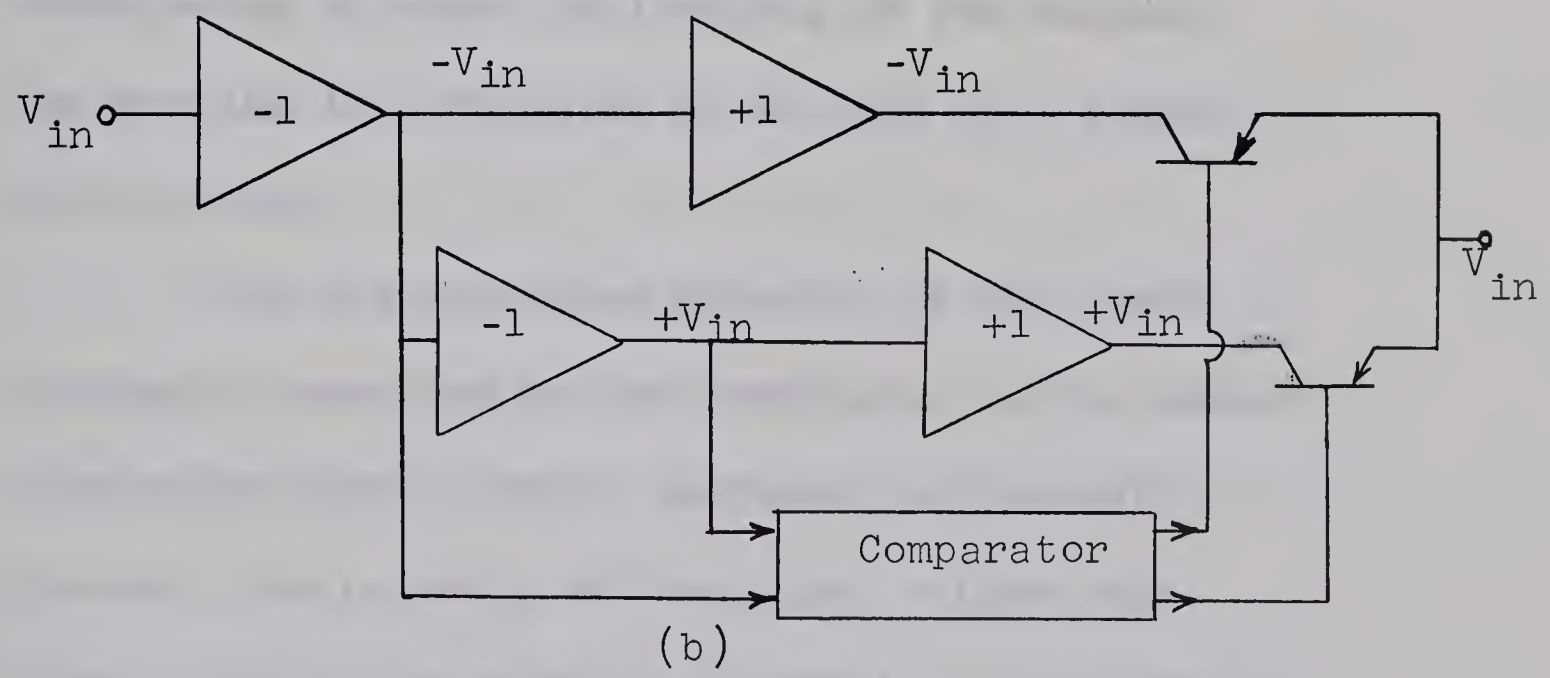


Only one approach to an absolute value circuit was found which would switch in a sufficiently short time to keep this error acceptably small. As shown in Fig. 5(a), it requires the use of another operational amplifier at the input to the encoder so that both $+V_{in}$ and $-V_{in}$ are available. Each amplifier has a transistor switch in series with its output; these switches are controlled by a fast, sensitive comparator such that the switch connected to the amplifier with the positive output voltage is conducting, while the other switch is off. Combining the outputs of the two switches produces the absolute value of the input voltage.

At the instants these series switches turn on and off, a rapid step change occurs in the output current of the operational amplifiers which causes an oscillatory transient on the output of each operational amplifier. The reason for this transient is that, because of the feedback around the amplifier, its output impedance appears to have an inductive component. Since the output of each operational amplifier is also connected to the comparator, this transient causes the comparator to switch between its two states. Each time it switches a new tran-



(a)



(b)

Figure 5. Block Diagram of Absolute Value Circuit

sient is generated, and there exists the possibility of continuous oscillation in the circuit of Fig. 5(a) when V_{in} is near zero volts. This situation is prevented by interposing a unity gain amplifier between each operational amplifier and the corresponding transistor switch, as shown in Fig. 5(b); the tran-

sients are then isolated from the inputs of the comparator, and the system is stable.

If the simple encoder of Fig. 3 were used to encode a time-varying voltage, the voltage actually encoded would not be the value at the instant the trigger pulse initiated the encoding process, but the value at some later time (when the ramp voltage is equal to the input voltage). This would result in sampling at irregular intervals, which would be troublesome in some applications of the encoder. The problem is eliminated by the use of a sample-hold circuit.

The instantaneous polarity of the input voltage is provided by the comparator in the absolute value circuit which operates continuously. However, the polarity of the input voltage may change during the encoding interval. At the end of the conversion the magnitude of the voltage held in the sample-hold circuit is read out, but the polarity as indicated by the comparator may be incorrect, causing an appreciable error. The polarity of the input voltage must be sensed at the instant the sample-hold circuit begins its holding action, and this information must be held during conversion un-

til the encoded voltage is read out. This requires a flip-flop to hold the polarity information and a gate which allows it to change state only at the instant the sample-hold circuit begins to hold.

Another difficulty arises in connection with the oscillator and its gate. For a constant input voltage the time interval defined by the two comparator pulses is of constant length. However, if a free-running oscillator is gated by these pulses, there will be an uncertainty of one count in the binary counter. This effect can be seen by considering Fig. 6; the time intervals A and B are identical in duration, but interval A contains five negative-going edges which would trigger the counter, while interval B contains only four. To avoid this uncertainty

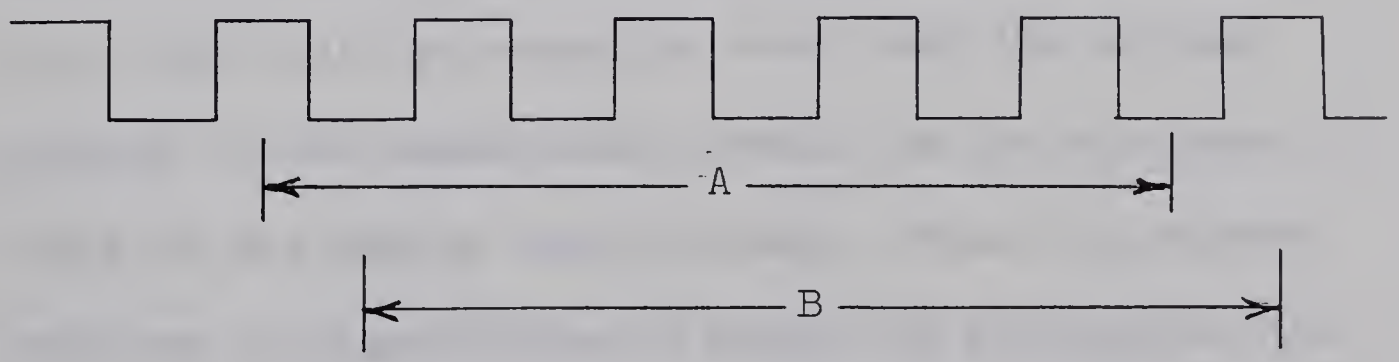


Figure 6. Counter Uncertainty

a gated oscillator, which is turned on and off by the comparator pulses, is used. This oscillator

must always start in the same way and with an initial amplitude large enough to trigger the counter at the end of the first cycle; these requirements indicate the use of a digital-type pulse generator rather than a sinusoidal oscillator.

In addition, a reset pulse generator is required to reset the flip-flops in the counter before each conversion. Two additional multivibrators are used to control the ramp generator and the sample-hold circuit.

A block diagram of the entire system, incorporating all the above refinements, is shown in Fig. 7. Briefly describing its operation, the input amplifiers, transistor switches and the polarity comparator function continuously. The polarity comparator ensures that the transistor switch, which has a positive input voltage, conducts such that the voltage applied to the sample-hold circuit is the absolute value of the analog input voltage. When the encoder receives a trigger pulse to begin the conversion, the sample-hold circuit samples this voltage for 1.5 microseconds. As it begins to hold, it enables the gate, which allows the polarity flip-flop to change state, if necessary, such that it correctly represents

the polarity of the analog input voltage at the instant the sample was taken. At the same time the ramp generator is triggered; however, the amplifier used in the ramp generator is initially saturated and the ramp voltage is clamped at + 10.4 volts. There is a delay of approximately 1.5 microseconds while the amplifier recovers from saturation and the ramp reaches +10 volts. During this period the reset pulse generator is triggered, which resets all the flip-flops in the counter immediately before the encoding of the new sample begins.

When the ramp voltage is equal to the voltage held by the sample-hold circuit, comparator A generates a step which starts the gated oscillator, and the counter begins to count the oscillator pulses. When the ramp voltage is zero, the step from comparator B stops the oscillator. The oscillator frequency is chosen such that during each cycle the ramp voltage changes by ten millivolts; thus the number held in the counter is the number of ten millivolt steps needed to reproduce the input voltage. This number can then be read out, 20 microseconds after the external trigger signal began the conversion. As the ramp voltage becomes negative, it actuates

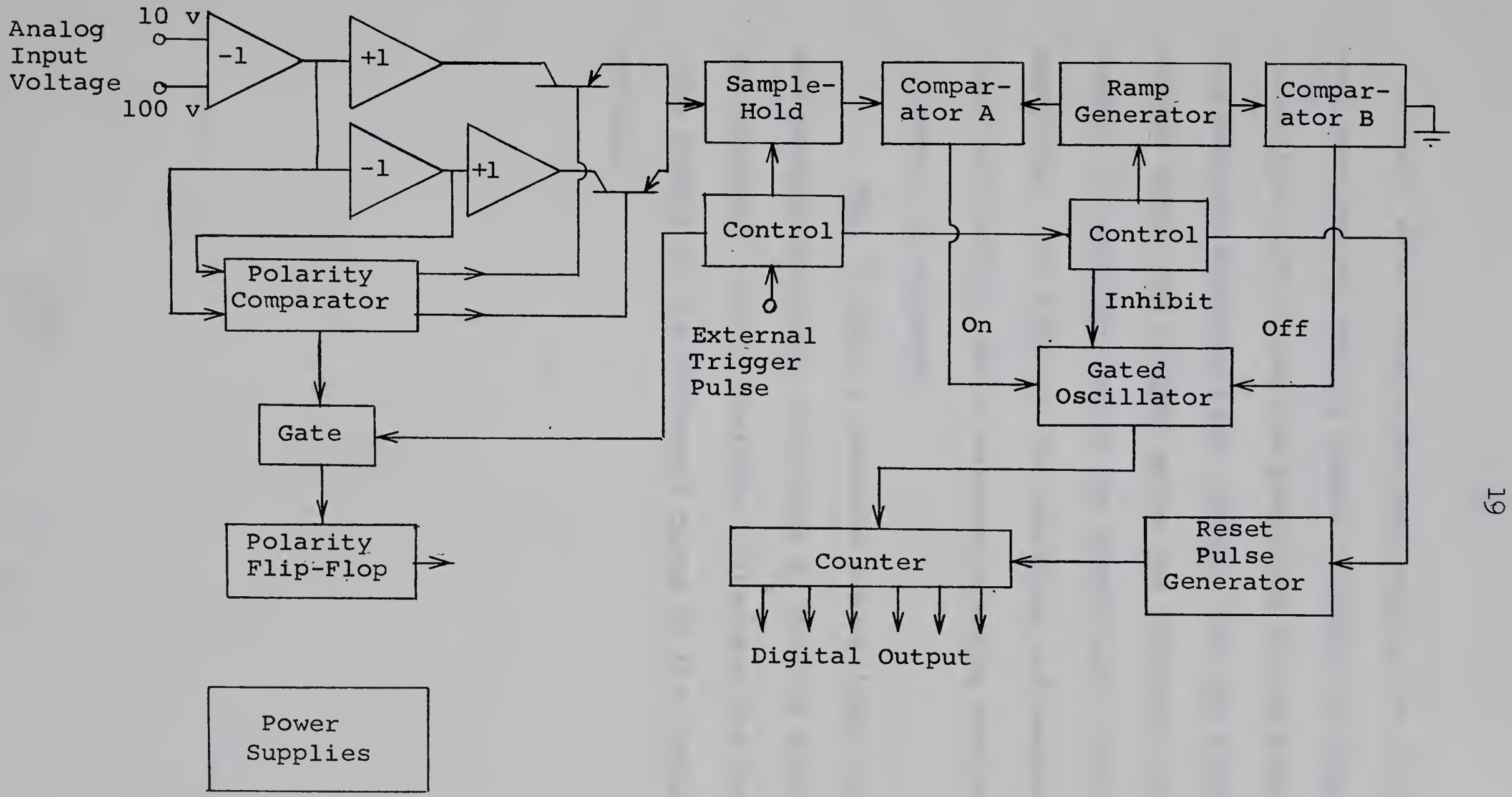
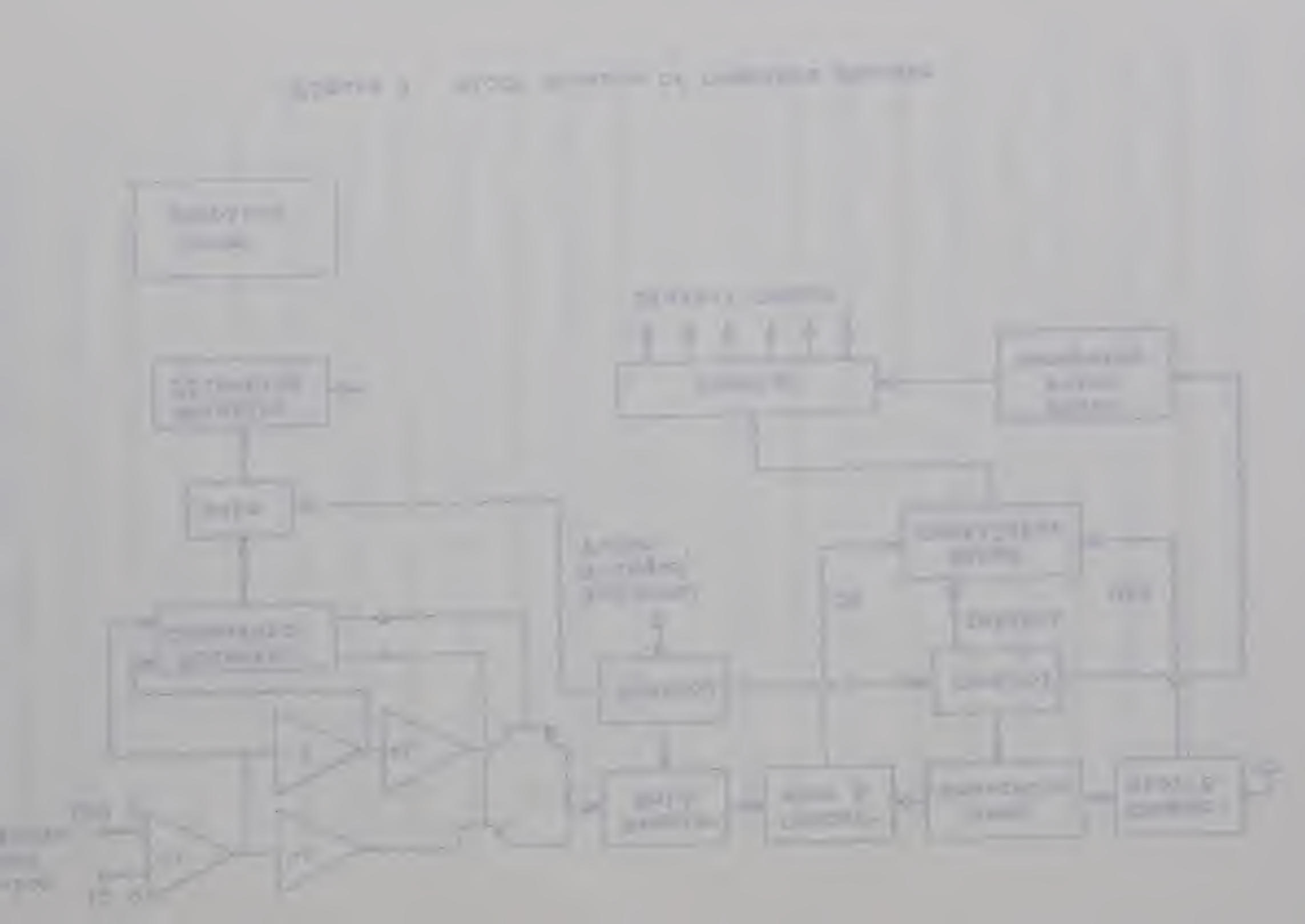


Figure 7. Block Diagram of Complete Encoder



a circuit which resets the ramp voltage to +10.4 volts, and provides an inhibit signal required to keep the oscillator off during the resetting of the ramp. At the maximum encoding rate, readout for one sample occurs after the trigger pulse for encoding the next sample is received (while the sample-hold circuit is sampling). In this way the encoding and readout periods can overlap, and a maximum encoding rate of 50 kilohertz is achieved.

Fig. 8 shows a possible analog input voltage and several pertinent waveforms at various points in the encoder. These waveforms illustrate the relative timing of the different parts of the conversion process.

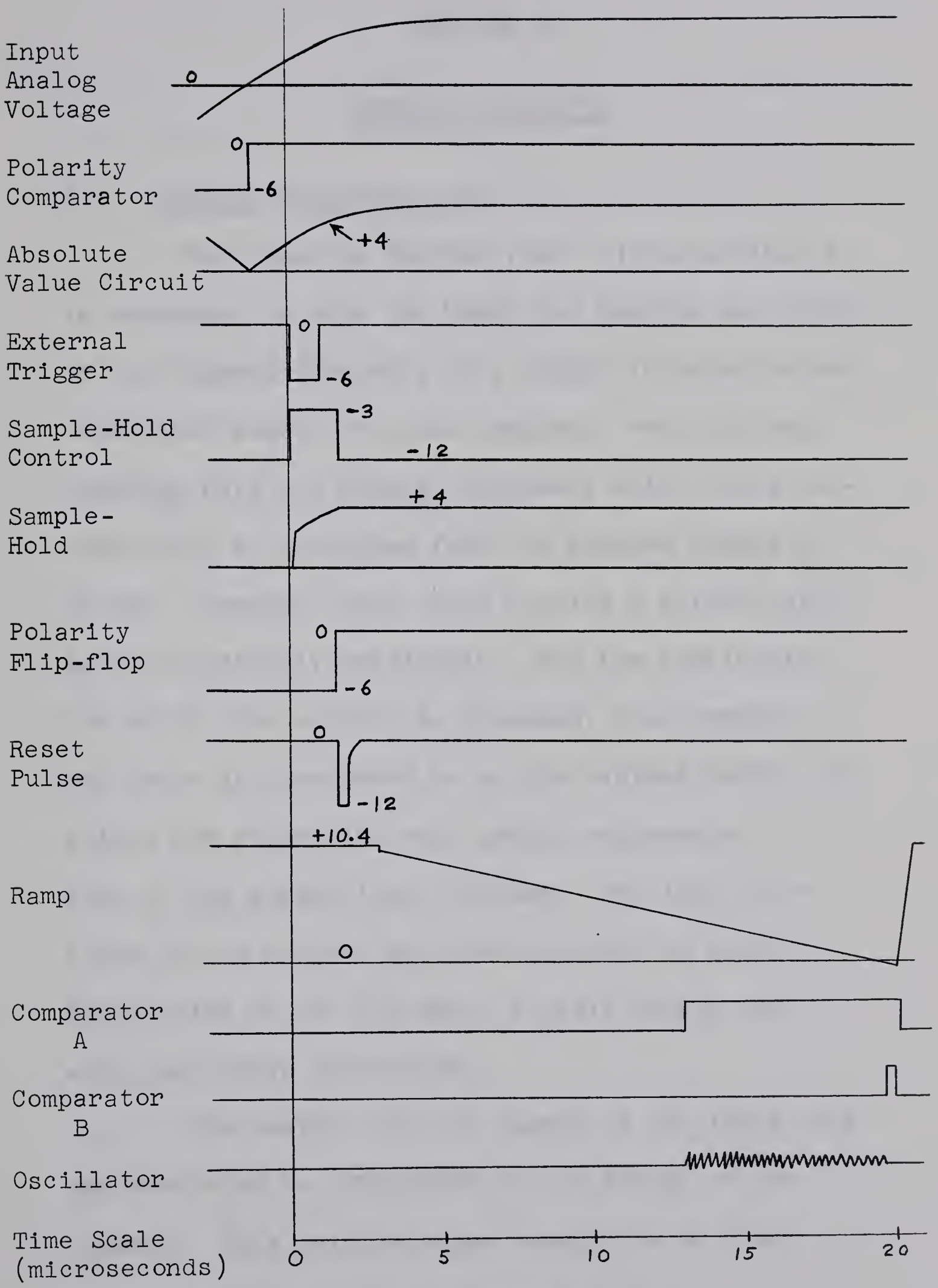


Figure 8. Typical Waveforms

CHAPTER 3

DETAILED CIRCUITS

3.1. General Considerations

The Sampling Theorem (Ref. 6) states that it is necessary to take at least two samples per cycle of the highest frequency in a signal in order to recover that signal from the samples. For a 50 khz. encoding rate the highest frequency which could theoretically be recovered from the sampled signal is 25 khz. However, this would require a filter which is not physically realizable. For the application for which this encoder is intended, four samples per cycle is considered to be the minimum number required for recovering any useful representation of the analog input voltage. The input circuits of the encoder are then required to handle frequencies up to 12.5 khz., at full output and with negligible distortion.

The maximum rate of change of the input voltage must also be considered in the design of the encoder. This maximum slope occurs for an input sine wave which can be represented by

$$V_{in} = V_m \sin 2\pi ft$$

where V_m = 10 volts and f = 12.5 khz. Differentiating this expression gives the maximum rate of change as

$$\left(\frac{dV_{in}}{dt}\right)_{max.} = 2\pi f V_m \cos 2\pi ft \Big|_{t=0}$$

$$= 2\pi f V_m = 78.5 \times 10^4 \text{ volts per second.}$$

This result is used later in the discussion of the absolute value circuit.

3.2. The Operational Amplifier

The D. C. amplifier circuit used in the two operational amplifiers is shown in Fig. 9. A differential amplifier with matched transistors is used for the input stage to obtain low temperature drift. Diodes D_1 and D_2 limit the summing junction voltage when the amplifier is overloaded, protecting Q_1 and Q_2. R_{10} provides base current for Q_2, decreasing the amplifier input current. The amplifier balancing network (R_1-R_5) is used to set the amplifier output voltage to zero when the input is grounded; it has a range of $\frac{+1}{-4}$ volt at the output when the amplifier is used as a unity-gain operational amplifier, and has a negligible effect on the amplifier open-loop gain and frequency response. Transistor Q_3 provides only a small amount of gain, but it isolates the two frequency

compensation networks (C_1, R_7 and R_8, and C_3 and R_{12}). Most of the open-loop gain is provided by Q_4 and Q_5, connected as a positive gain compound transistor. R_{14} has little effect on the normal operation of the amplifier, but it protects Q_4 from excessive power dissipation in the event of an amplifier overload.

To obtain sufficient output current and voltage swing without drawing excessive power supply current or employing a power transistor for an output emitter follower, a complementary emitter follower is used as the output stage. R_{17}, R_{20}, D_3 and D_4 supply the proper bias for Q_6 and Q_7. R_{18} and R_{19} are necessary to reduce the limiting effect on the output voltage swing due to D_3 and D_4 cutting off when the output voltage approaches +10 or -10 volts. R_{21} and R_{22} cannot be made large enough to protect Q_6 and Q_7 against a sustained short circuit on the output without reducing the output voltage swing, but they provide some degree of protection against momentary shorts.

The two frequency compensation networks shape the frequency response to obtain closed-loop stability when the amplifier is used as a unity-gain inverter. However, the size of capacitors used affects the max-

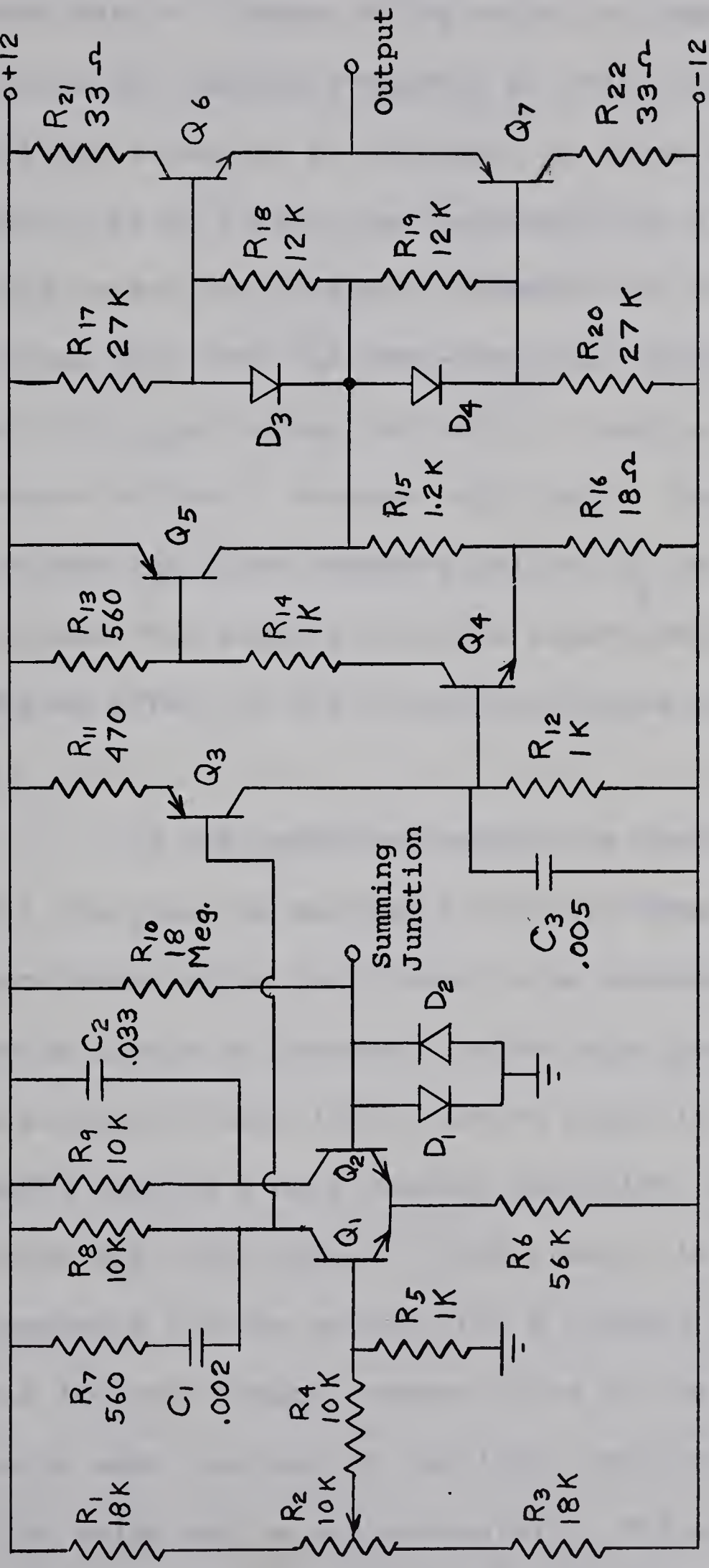
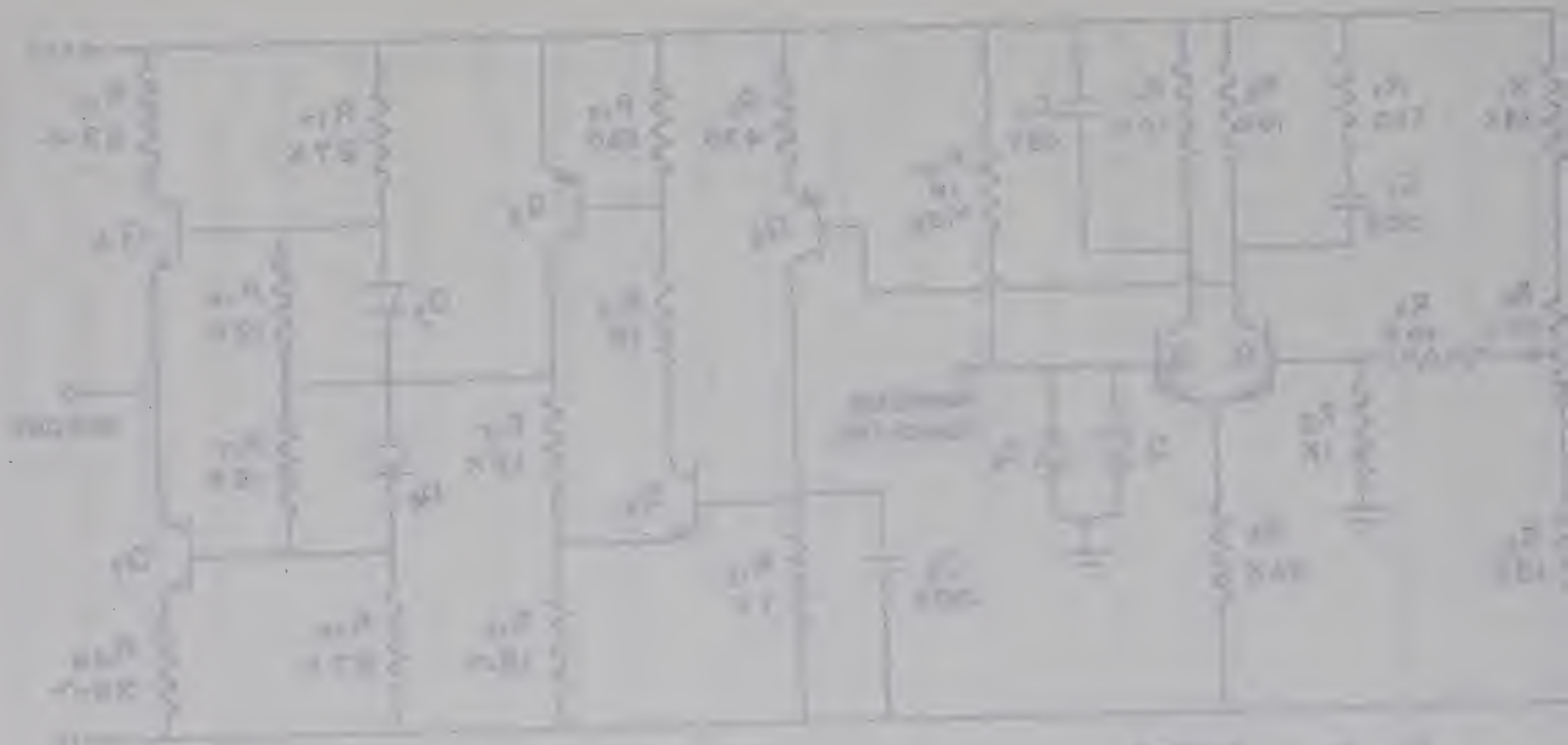


Figure 9. Operational Amplifier



imum rate of change of the output voltage, and therefore limits the maximum frequency at which the full output voltage swing can be obtained, so these capacitors should be no larger than necessary for stability. For this reason the frequency compensation networks are chosen such that the open-loop gain decreases at a rate of 40 db. per decade initially, changing to 20 db. per decade before it reaches unity gain. Capacitor C_2 decreases the high-frequency gain of Q_2 in order not to increase the summing junction capacitance by the Miller effect on the collector-to-base capacitance of Q_2.

If the amplifier werecto be used at a gain of 0.1 (to give the encoder a 100 volt range) the 20 db. per decade slope would have to be extended over an extra decade of frequency below unity gain, for reasons discussed in Ref. 10, to ensure stability. Since this would require a more complex amplifier, an input attenuator was used instead. This results in a lower input impedance for the encoder (45 K instead of 100 K) on the 100 volt range; however, this is adequate. Adjustments were included on the input resistors so the amplifier gains can be set accurately. The arrangement of input and feedback resistors used on the two operational

amplifiers is shown in Fig. 10.

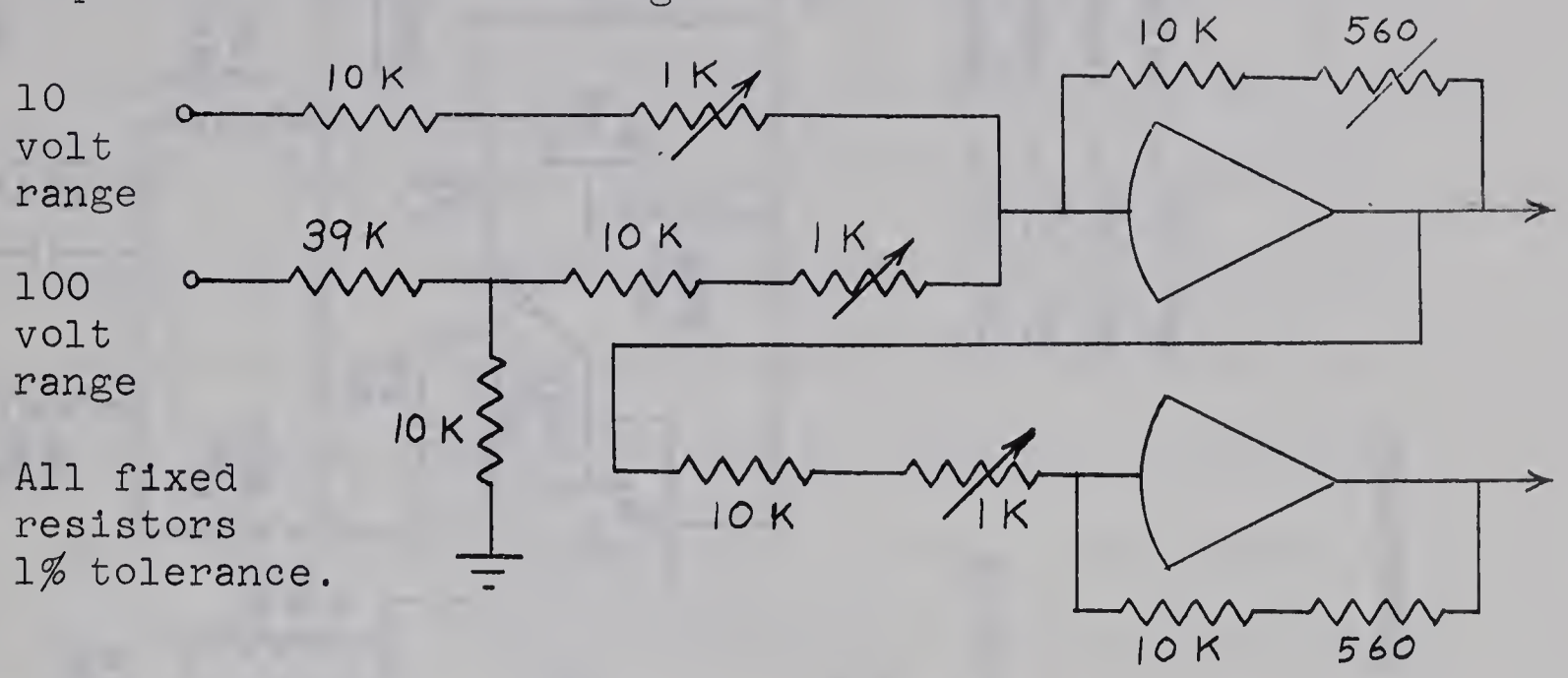
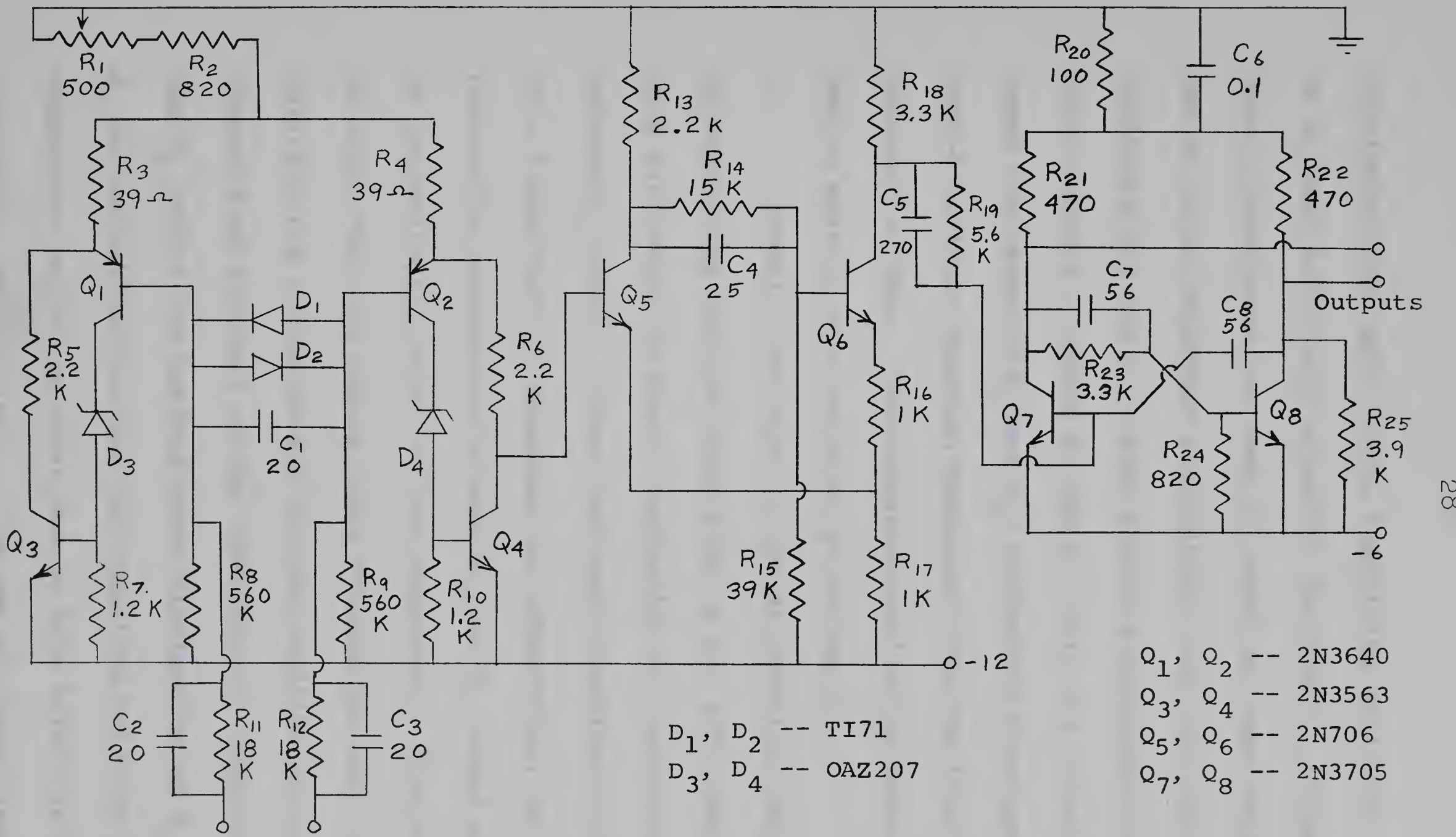


Figure 10. Input and Feedback Resistors

The open-loop gain of the amplifier is approximately 2000. Used as a unity gain inverter, the amplifier delivers an output voltage swing of $\pm$10.4 volts into a 5K load at frequencies up to 20 khz. The maximum rate of change of the output voltage is 2 volts per microsecond, which is much greater than for any waveform from the computer with which the encoder is to be used.

3.3. The Polarity Comparator

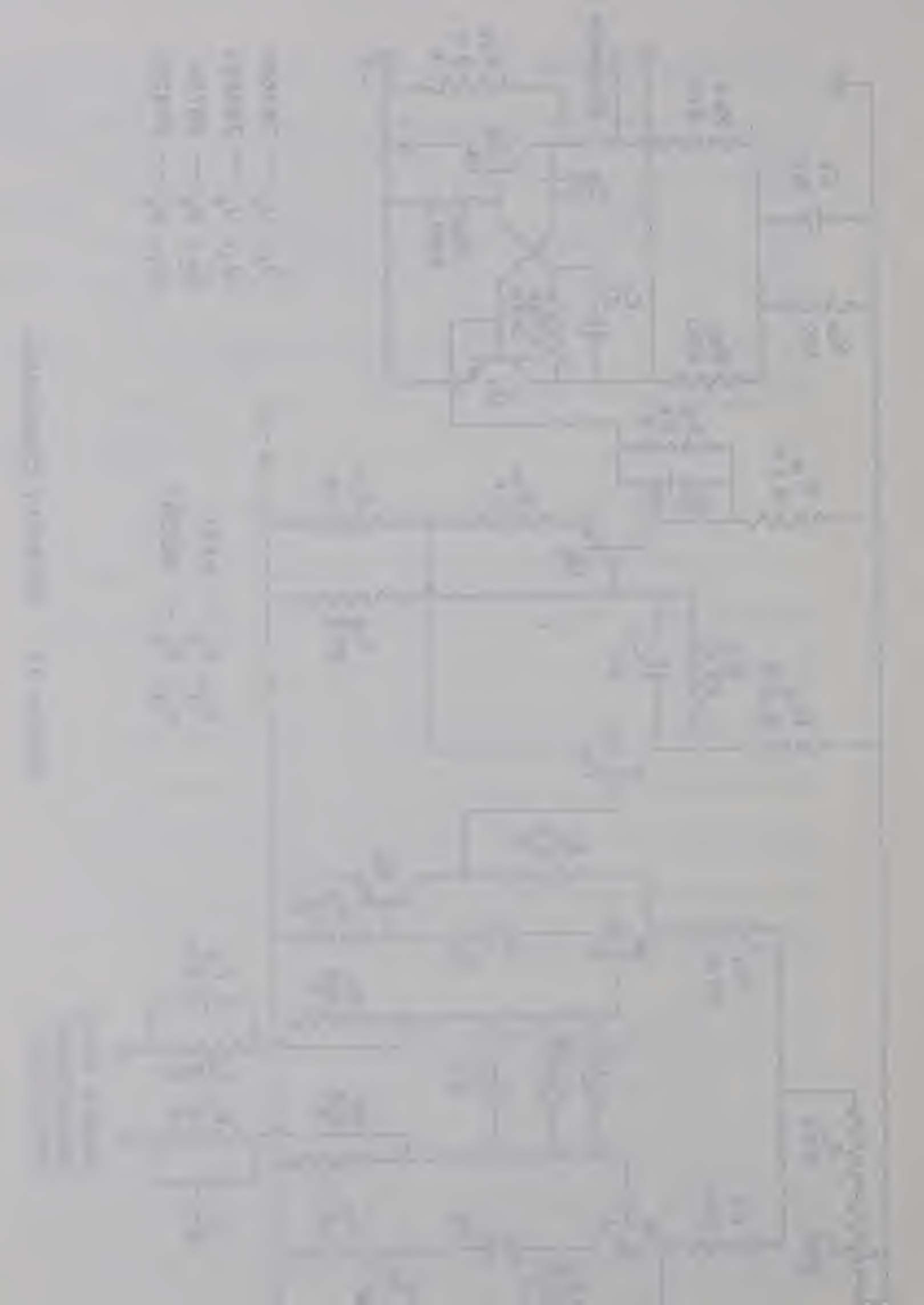
The function of the polarity comparator, shown in Fig. 11, is to provide a continuous indication of the polarity of the analog input voltage, as well as to supply two complementary outputs having the voltage levels required to operate the absolute value circuit. The input differential stage provides a differential-



D_1, D_2 -- TI71
D_3, D_4 -- OAZ207

Q_1, Q_2 -- 2N3640
Q_3, Q_4 -- 2N3563
Q_5, Q_6 -- 2N706
Q_7, Q_8 -- 2N3705

Figure 11. Polarity Comparator



to-single-ended gain of 50, amplifying millivolt signals to a level sufficient to switch the Schmitt trigger. Compound transistors are used to obtain a large bandwidth and an input impedance sufficiently high that the input resistors R_{11} and R_{12} cause little attenuation for small input signals. Diodes D_1 and D_2 limit the voltage between the bases of Q_1 and Q_2, protecting them against base-to-emitter junction breakdown when the input analog voltage is large. The comparator switching point can be set to exactly zero volts by adjusting R_1.

Normally one side of the differential amplifier is conducting and the other side is cut off, resulting in a difference in power dissipation and temperature between Q_1 and Q_2. Since the base-to-emitter voltage of a transistor is dependent on temperature, any difference in temperature between Q_1 and Q_2 causes a drift in the switching point of the comparator. This effect is worst when the analog input voltage has been of one polarity for a long period of time relative to the thermal time constant of the transistors. Zener diodes D_3 and D_4 reduce the maximum power dissipation of Q_1 and Q_2 to two milliwatts, and the resulting drift of the comparator switching point due to this effect is approximately one millivolt. The use of Zener diodes

also avoids the loss of bandwidth which would be incurred if resistors were used instead to reduce the collector voltages of Q_1 and Q_2. The use of resistors would allow saturation of these transistors, and the accompanying increase in turn-off delay would further increase the switching time of the comparator.

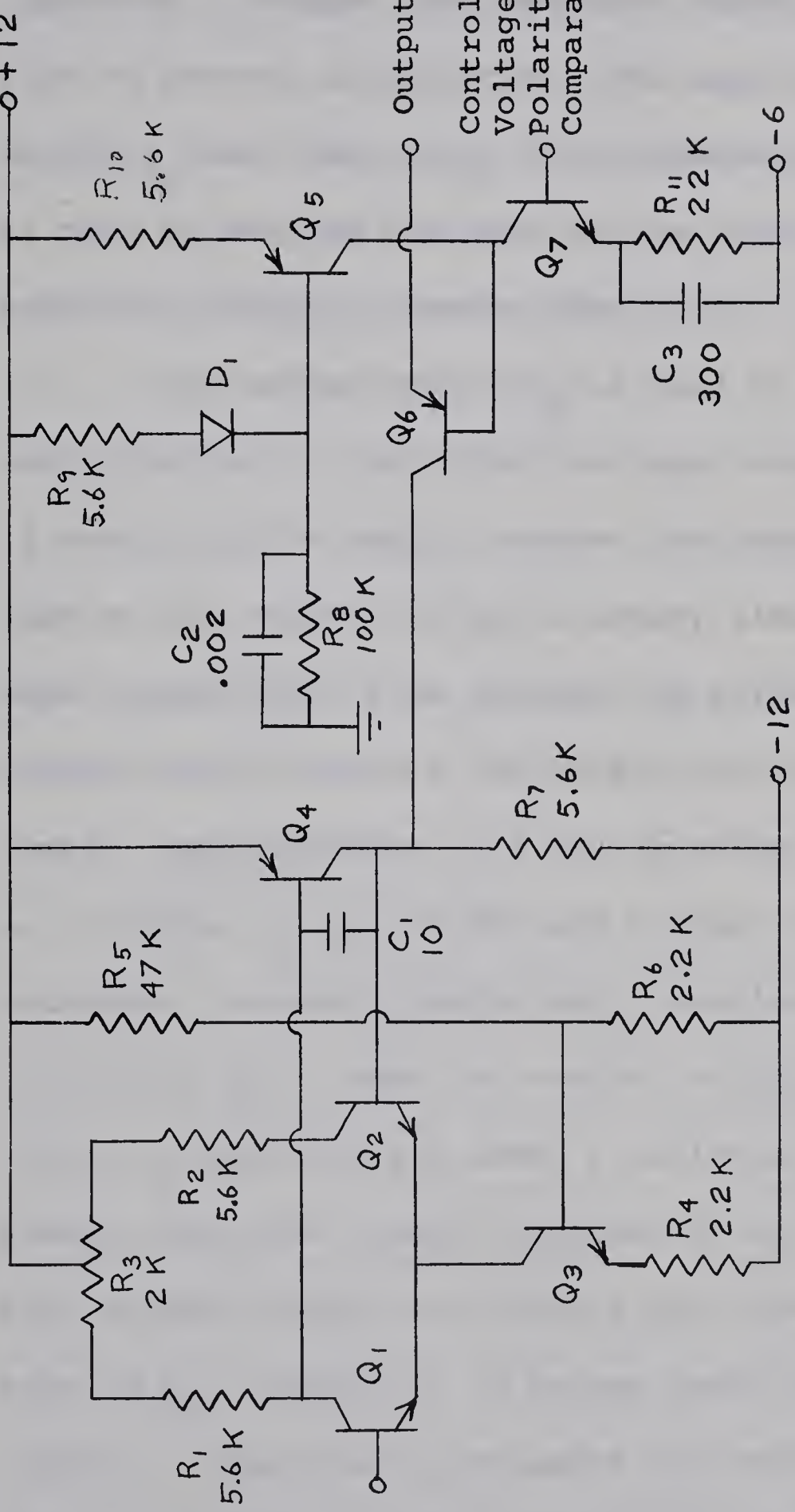
The input amplifier is followed by a Schmitt trigger circuit designed for low hysteresis between the switching voltage levels, this hysteresis being further reduced by the inclusion of R_{16}. The output flip-flop, used to provide the complementary output signals required by the transistor switches in the absolute value circuit, is DC-coupled to the Schmitt trigger. R_{20} decreases the more positive output voltage level to -1.6 volts, as required by the transistor switches. R_{25} provides a load on the collector of Q_8 similar to the effect of R_{23} and R_{24} on the collector of Q_7, so the output voltage levels on the two outputs are equal.

After the polarity comparator was constructed it was found that, for input voltages very near zero volts, there was a tendency for the comparator to switch continuously between its two states, due to the switching transient generated each time the comparator changed state and to pickup of radio frequency inter-

ference. This effect was greatly reduced by the addition of capacitor C_1 between the bases of the input transistors, decreasing the high-frequency gain of the input stage. C_1 cannot be made large enough to eliminate completely this effect without increasing the switching time of the comparator, but the small amount remaining is not objectionable. The comparator switches state within 80 nanoseconds after the input voltage crosses zero, for any amplitude of signal within the range of the encoder and for any frequency below 12.5 khz.

3.4. Absolute Value Circuit

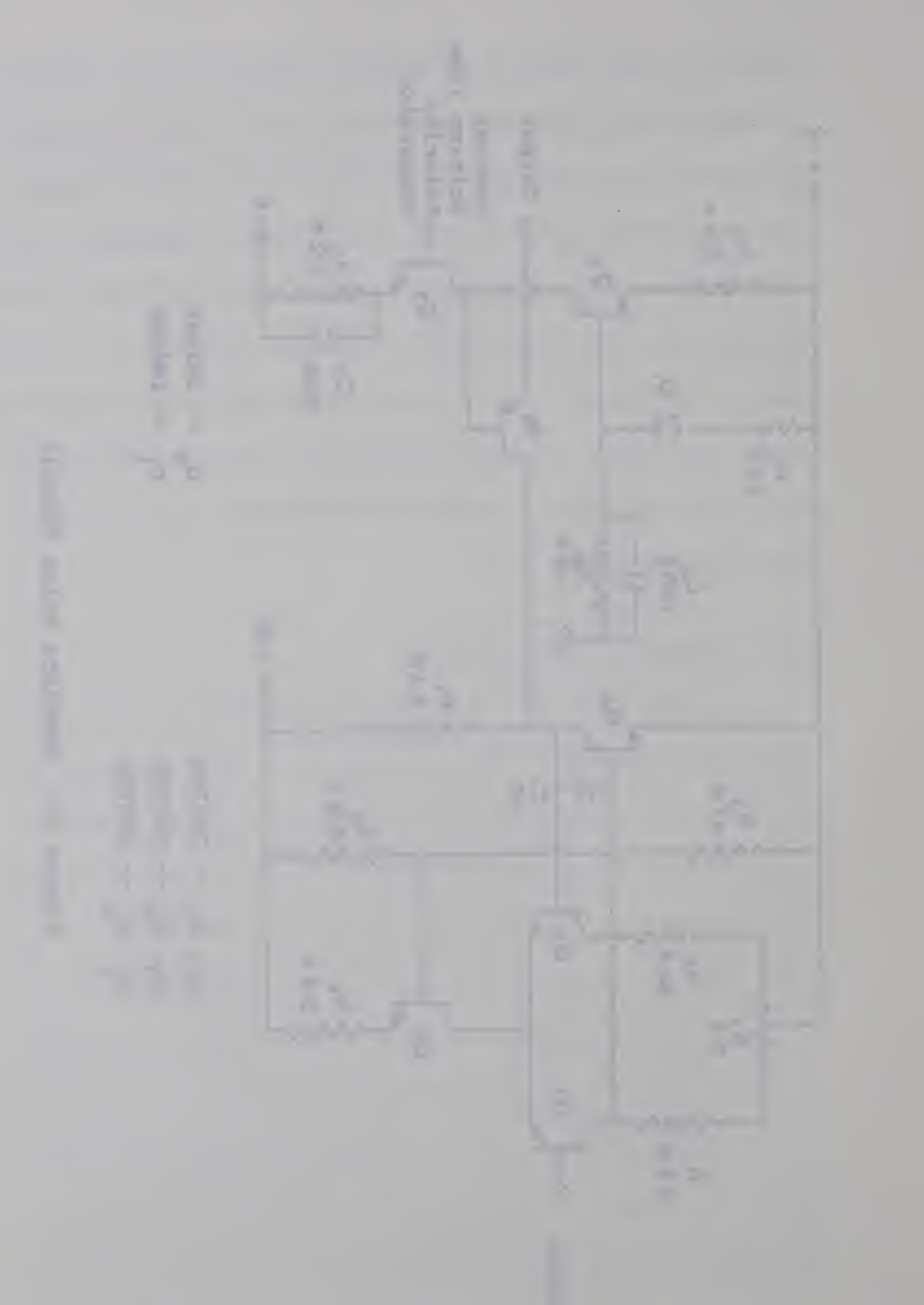
The absolute value circuit consists of two identical parts like that shown in Fig. 12. Each is made up of a unity gain amplifier and a series transistor switch, connected as shown in Fig. 5(b). In the unity gain amplifier the input stage (Q_1 and Q_2) is a differential amplifier used to obtain good temperature stability. Current source Q_3 is necessary because of the large common-mode voltages applied to the differential stage in this amplifier configuration. R_3 is a balancing adjustment which provides a means of cancelling the offset voltage in the amplifier and the series switch; it can be set to cancel the offset voltage in the sample-hold circuit



Q_6 -- 2N2945
D_1 -- 1N456A

Q_1, Q_2 -- 2N3704
Q_3, Q_4 -- 2N3705
Q_5, Q_6 -- 2N3702

Figure 12. Absolute Value Circuit



as well, if this is large enough to be objectionable. Capacitor C_1 shapes the frequency response of the amplifier to prevent oscillation. The amplifier gain is slightly less than unity, but compensation for this can be made by setting the gain of the input operational amplifier slightly greater than unity.

The series switch Q_6 is used in the inverted configuration so the offset voltage across it when it is conducting is small; because the impedance of the load on the emitter of Q_6 is large, almost all of the base current must flow through the collector. The voltage which controls the switch can have only two levels, approximately -1.6 and -6 volts. When it is at -6 volts, Q_7 is cut off and current source Q_5 saturates, reverse biasing both junctions of Q_6 and cutting it off. When the control voltage is at -1.6 volts, Q_7 conducts and draws a collector current greater than the current supplied by Q_5. The difference between these two currents must come from the base of Q_6, causing it to become practically a short circuit. Capacitor C_3 bypasses the emitter resistor of Q_7, providing a large transient current to turn Q_6 on and thereby decreasing its switching time. Current sources Q_5 and Q_7 are used in order to

maintain a constant base current for Q_6, independent of the analog input voltage; the offset voltage across Q_6 when it conducts is then a constant two millivolts, and R_3 may be adjusted to compensate for it.

A type 2N2945 transistor was chosen for Q_6 because of its high base-to-emitter breakdown voltage, since this junction may be subjected to a reverse bias of 22 volts. Unfortunately this requires a relatively thick base region in the transistor which increases its switching time, resulting in a total switching time for the polarity comparator and the absolute value circuit of 0.2 microsecond.

3.5. Sample-Hold Circuit

The sample-hold circuit shown in Fig. 13 is activated by the external trigger pulse, which triggers a monostable multivibrator (Q_2 and Q_3). It generates a 1.5 microsecond pulse, causing a sample of the voltage from the absolute value circuit to be taken. Q_1 provides an output having the proper voltage levels to operate the polarity bit circuit, enabling the polarity bit to change if necessary. Diode D_1 is required to prevent breakdown of the base-emitter junction of Q_2, with the consequent

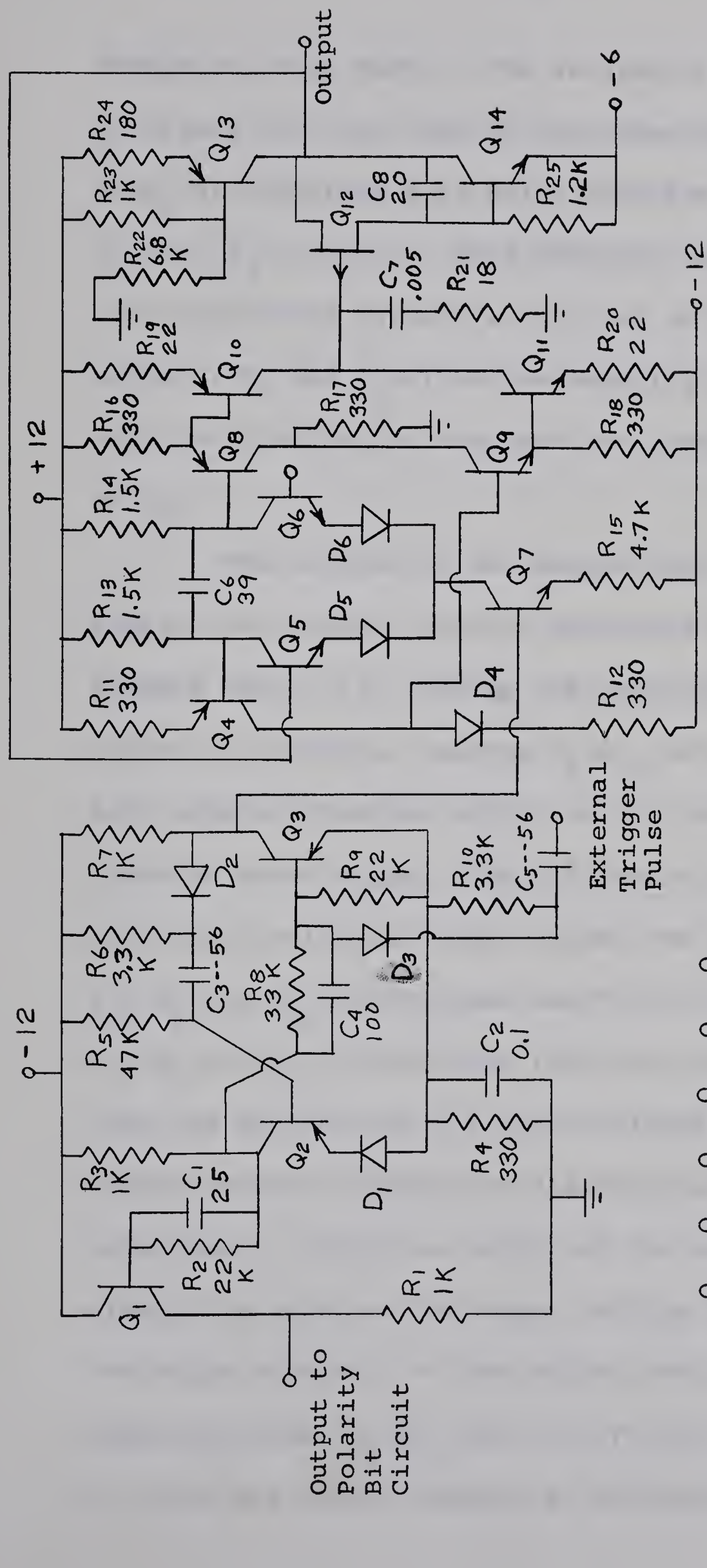


Figure 13. Sample-Hold Circuit.

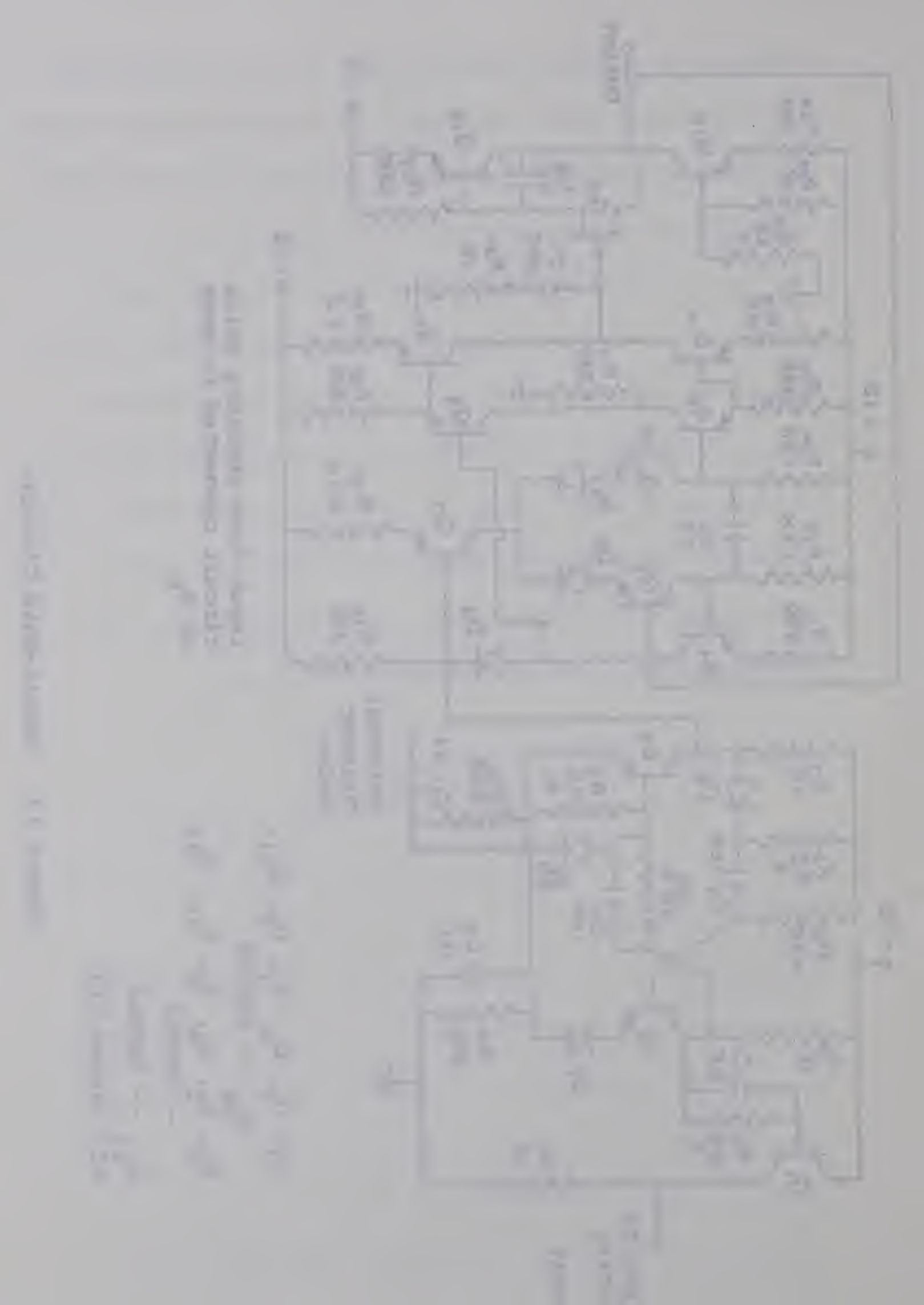
Input from absolute value circuit connected to base of Q_6.

Q_1, Q_5, Q_6, Q_7, Q_9, Q_{11}, Q_{14} -- 2N3704

Q_2, Q_3, Q_4, Q_8, Q_{10}, Q_{13} -- 2N3702

Q_{12} -- 2N2844

All diodes TI71



change in pulse width. The inclusion of D_2 and R_6 decreases the fall time of the pulse on the collector of Q_3 by isolating this point from the timing capacitor C_3 when Q_3 cuts off. This provides rapid turnoff for the sample-hold circuit at the end of the sampling period. R_4 and C_2 allow the sampling pulse to rise only to -3 volts, as required for proper operation of Q_7.

The balance of the sample-hold circuit is similar to a boxcar circuit described by Harris and Simmons (Ref. 11). During the sampling pulse current source Q_7 conducts, causing Q_4-Q_{11} to conduct. Feedback applied from the output to the base of Q_5 provides an error signal (the difference between input and output voltages) which causes the currents in Q_6, Q_8 and Q_{10} to increase and the currents in Q_4, Q_5, Q_9 and Q_{11} to decrease (or vice versa, depending upon the polarity of the error voltage). This unbalance causes charging or discharging of the hold capacitor C_7 until the output of the sample-hold circuit is equal to the input voltage from the absolute value circuit. At the end of the 1.5 microsecond sampling pulse, Q_4-Q_{11} are cut off and the charge on C_7 holds the output voltage of the sample-hold circuit

constant.

The circuit is symmetrical in order to provide equally rapid charging and discharging of C_7. Q_{10} and Q_{11} can conduct sufficiently large transient currents to change the voltage across C_7 by ten volts (the worst-case condition) in one microsecond. D_5 and D_6 are required to prevent base-emitter junction breakdown of Q_5 and Q_6 which would cause the output of the sample-hold circuit to follow the input during the holding period, whenever the analog input voltage changed by more than a few volts between samples.

The hold capacitor is followed by a unity gain isolating amplifier in which a field effect transistor is used to obtain a high input impedance, in order to avoid the rapid discharge of the hold capacitor. Q_{12} and Q_{14} are used as a compound source follower, in which current source Q_{13} maintains a constant current through Q_{12} in order that its transconductance (and therefore the amplifier gain) remain practically constant. A gain less than unity and a small offset voltage in the amplifier are not disadvantageous because in this sample-hold circuit the hold capacitor is charged not to the input voltage, but to whatever voltage is necessary to make the out-

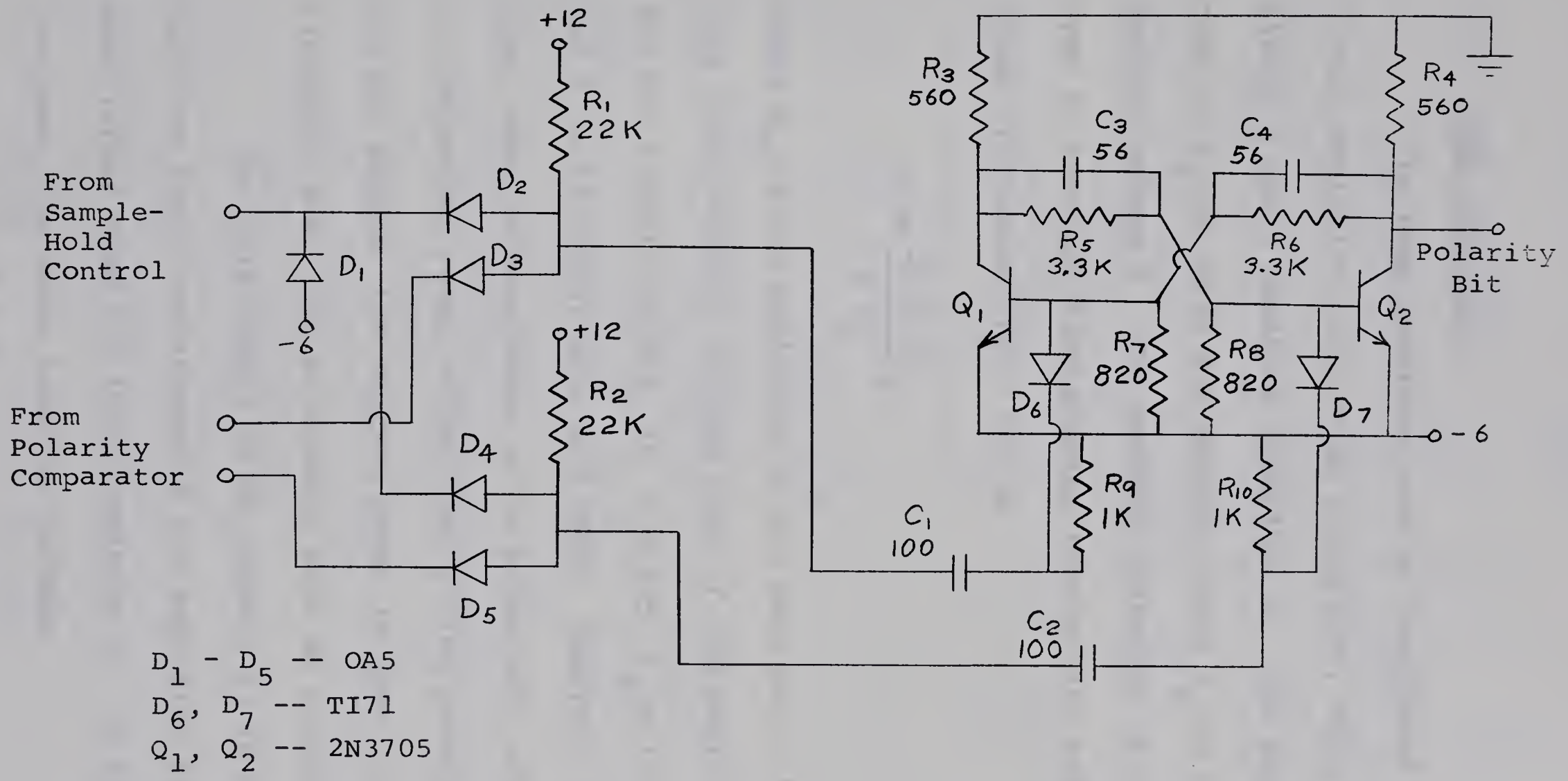
put voltage equal to the input voltage.

When the circuit is holding, capacitor C_7 is discharged slowly by the leakage currents of Q_{10}, Q_{11} and Q_{12}, causing the output to drift at a rate of 0.1 volt per second. In this application the output voltage is required to be accurate only during the first 18.5 microseconds of the holding period, so the error caused by this drift is entirely negligible. If a sample-hold circuit is required to hold a voltage for longer periods, this drift can be reduced greatly by the use of low-leakage diodes (as suggested in Ref. 10), a larger hold capacitor, and a MOSFET for Q_{12}. The temperature drift of the output amplifier due to changes in signal level can then be removed by adjusting R_{25}, setting the drain current of Q_{12} for zero temperature coefficient.

Calculation of the exact frequency response of the sample-hold circuit is difficult because of the presence of two forward signal paths and one feedback loop inside another. Capacitor C_8 is necessary to prevent oscillation in the output amplifier during the holding period, while C_6 and R_{21} are required to stabilize the closed-loop circuit during sampling.

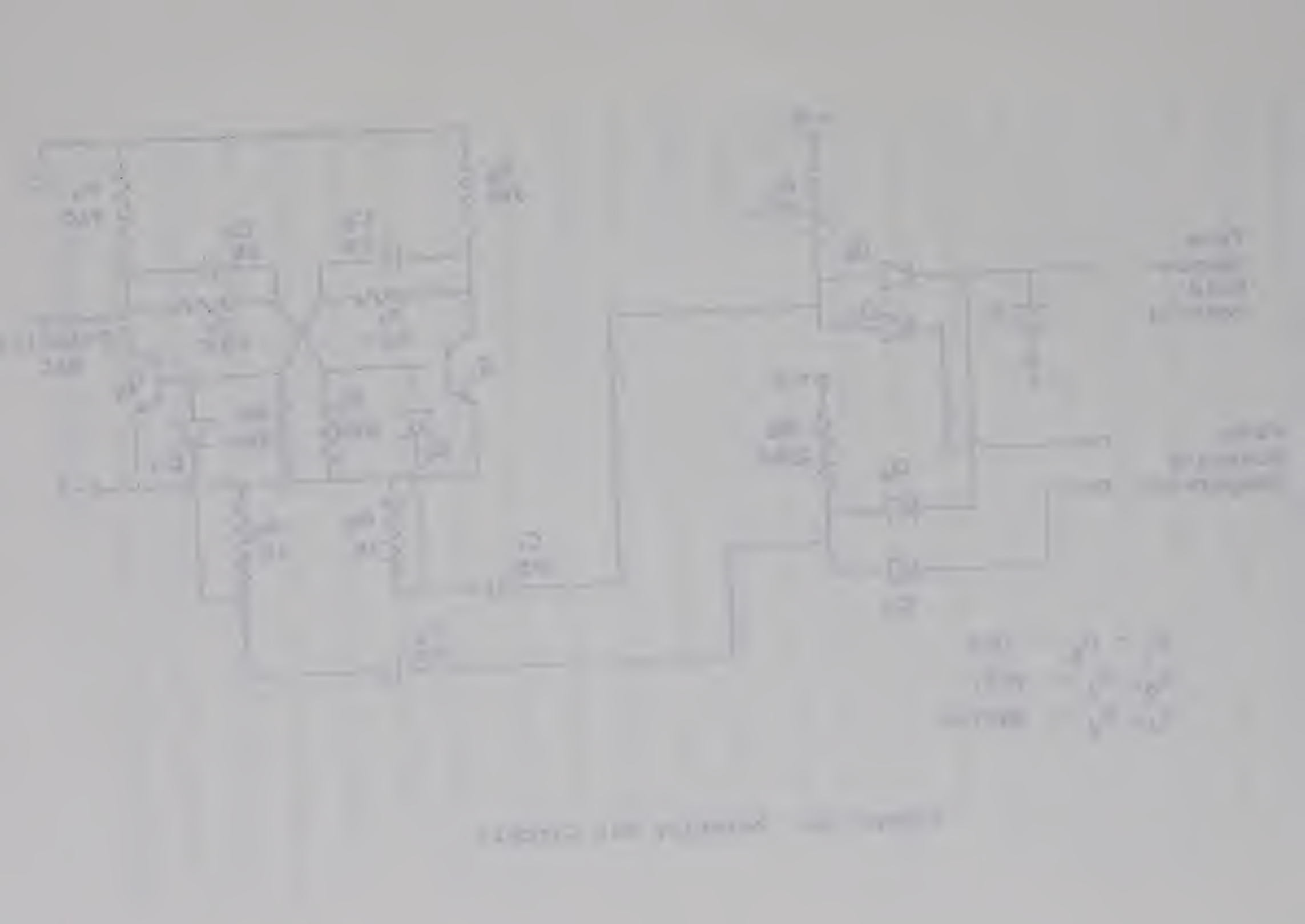
3.6. Polarity Bit Circuit

The circuit which stores the polarity information for each sample until readout occurs, shown in Fig. 14, consists of two diode AND gates and a flip-flop used in the set-reset mode. One or the other of the inputs from the polarity comparator is always at the -1.6 volt level, but the outputs of the gates remain at -6 volts until a pulse from the sample-hold control multivibrator is received, indicating that a new sample has been taken. Whichever gate has the -1.6 volt level at its other input transmits the sample-hold pulse to its output, where it is differentiated to produce two voltage spikes. Only the second of these, arising from the trailing edge of the sample-hold pulse, is of the proper polarity to trigger the flip-flop. Thus the flip-flop can change state only at the instant the sample-hold circuit begins to hold. As long as the analog input remains of one polarity, a train of pulses is applied to the base of one of the transistors in the flip-flop. However, only the first pulse after a change of polarity of the analog input voltage causes the flip-flop to change state; any later pulses to that base have no effect.



D_1 - D_5 -- OA5
D_6, D_7 -- TI71
Q_1, Q_2 -- 2N3705

Figure 14. Polarity Bit Circuit



3.7. Ramp Generator

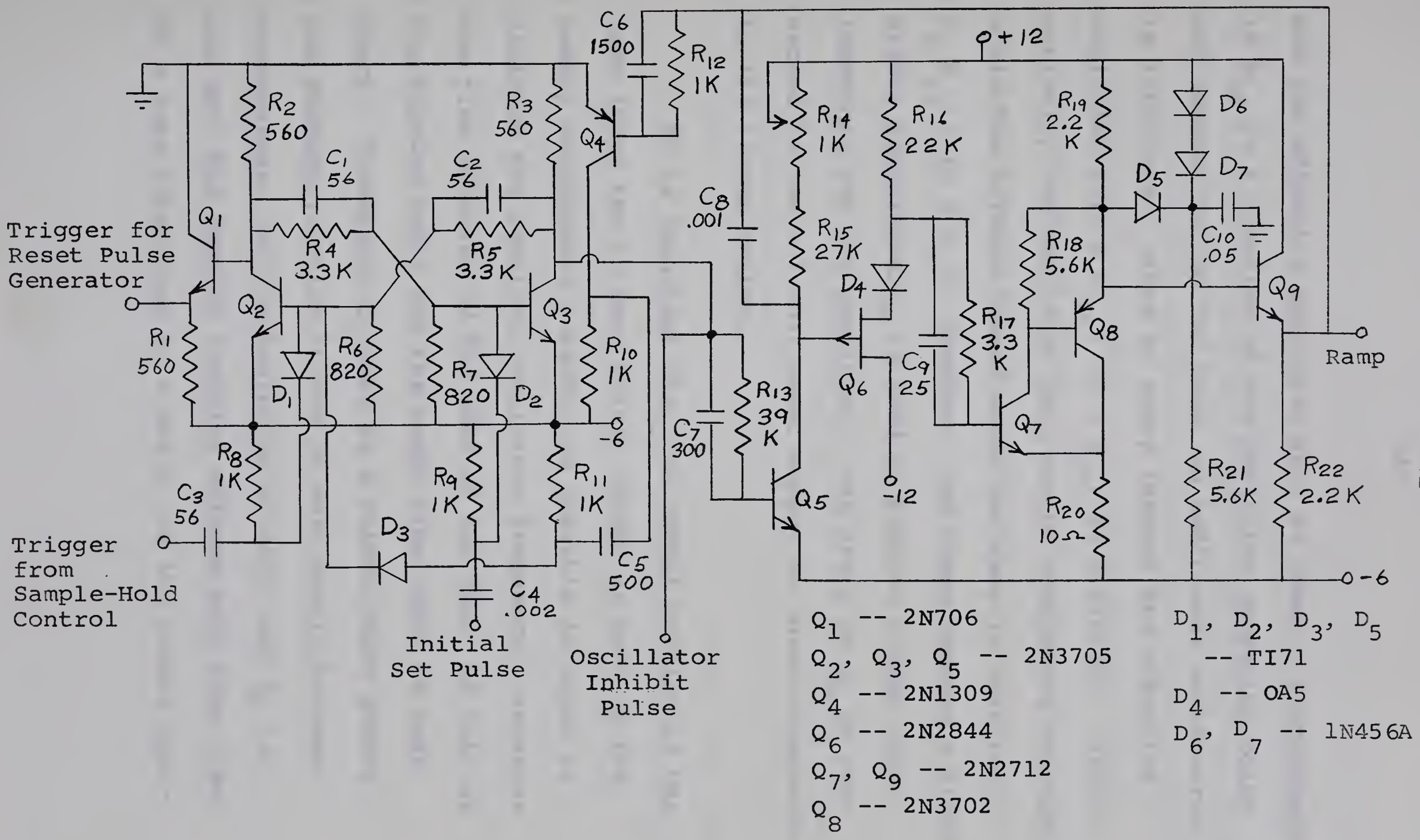
The ramp generator can be considered to be an operational amplifier used as an integrator, with an input resistor R and a feedback capacitor C. The slope of the ramp is V_s/RC volts per second, where V_s is the voltage applied across R. The maximum deviation (e) of a ramp from a straight line passing through its end points is given by Strauss (Ref. 12) as

$$e = \frac{12.5\ V_r}{A\ V_s}\%$$

where V_r is the amplitude of the ramp and A is the open-loop low frequency voltage gain of the amplifier used. For the circuit of Fig. 15, A = 155, V_s = 17.5 volts and V_r = 10 volts, so e = 0.046%. However, if the ideal ramp is considered to be a best-fit straight line to the actual ramp, rather than a line passing through its end points, the maximum error is then 0.023%, sufficiently small for an encoder with an accuracy of 0.1%.

For this result to be correct it is necessary that the input resistance of the amplifier (R_{in}) be much larger than the input resistor R. If this is not the case, the above equation becomes

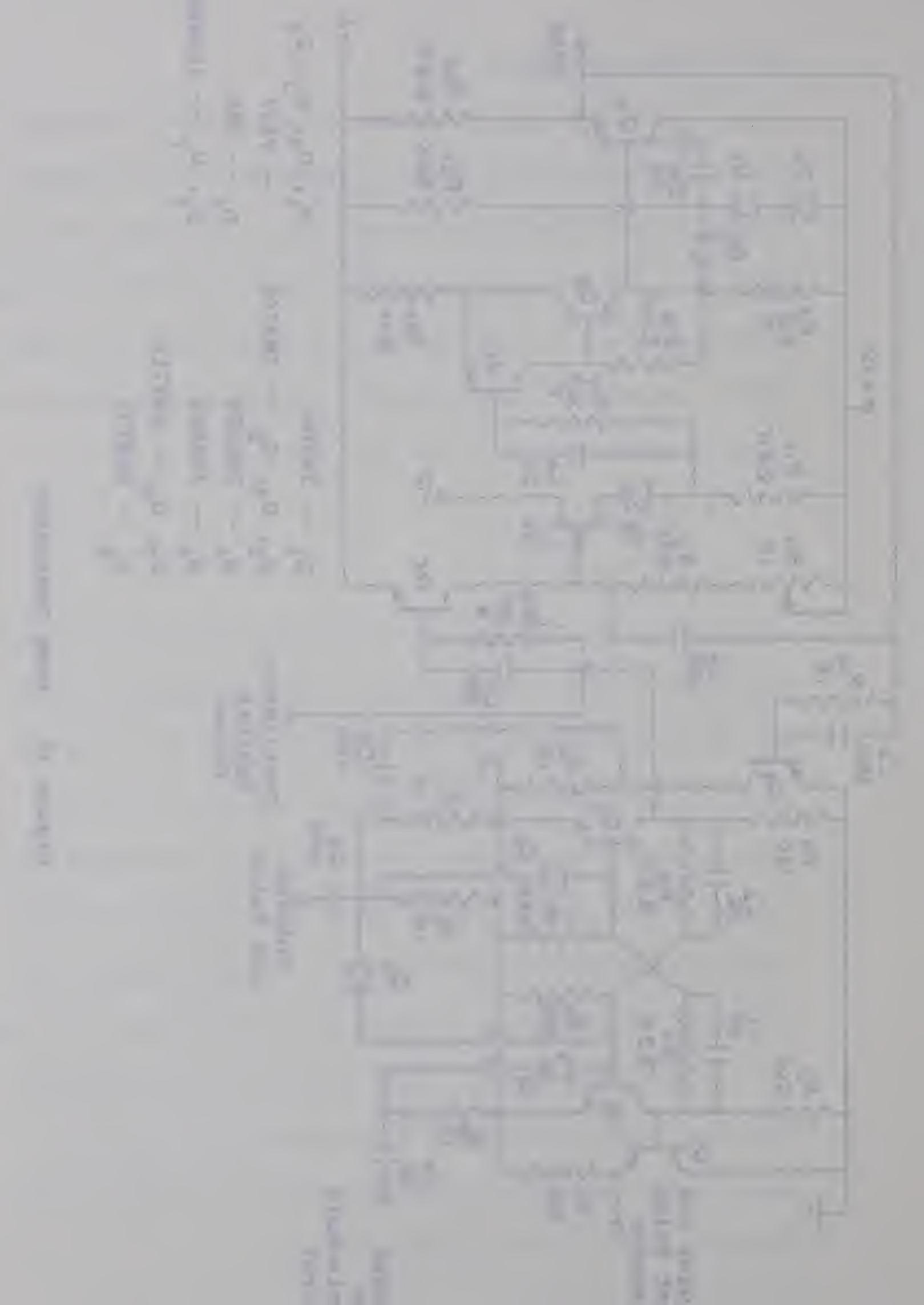
$$e = \frac{12.5\ V_r}{\frac{R_{in}}{R + R_{in}} A\ V_s}\%$$



Q_1 -- 2N706
Q_2, Q_3, Q_5 -- 2N3705
Q_4 -- 2N1309
Q_6 -- 2N2844
Q_7, Q_9 -- 2N2712
Q_8 -- 2N3702

D_1, D_2, D_3, D_5 -- TI71
D_4 -- OA5
D_6, D_7 -- 1N456A

Figure 15. Ramp Generator



and the effective amplifier gain is lower. Furthermore, if R_{in} is a function of the amplifier operating point and changes during the ramp, an additional nonlinearity is introduced, since at every instant the effective amplifier gain $A\ R_{in} / (R + R_{in})$ is different. Alternatively, the amplifier gain can be considered constant while the voltage toward which the ramp is charging, $V_s\ R_{in} / (R + R_{in})$, changes. For these reasons a field effect transistor Q_6 is used to provide a high input impedance for the amplifier. The drain of Q_6 is connected to the -12 volt power supply to ensure operation in its linear region.

It is important that the useful portion of the ramp (from ten to zero volts) occupy as much of the twenty microsecond interval as possible in order to minimize the required oscillator frequency; therefore the time occupied by the ends of the ramp, as well as the turn-on delay and the reset time, must be made short. Transistor Q_5 acts as a switch which shorts the summing junction to the -6 volt supply between conversions. At the beginning of each ramp Q_5 is cut off; the summing junction voltage must then rise, at a rate determined by R and C, to its normal oper-

ating voltage before the ramp can begin. In order to make this delay small, the circuit is arranged such that the summing junction voltage is approximately -5.6 volts during normal operation, rather than being at ground potential as is common in operational amplifiers. The gate-to-source voltage of Q_5 and the voltage across D_4 set the summing junction voltage to this point. In addition D_4 provides temperature compensation for the base-to-emitter voltage of Q_7. Since Q_5 is biased for zero temperature coefficient the summing junction voltage, and hence the initial turn-on delay, are relatively stable with respect to temperature changes. This is desirable because the reset pulse generator resets all the flip-flops in the counter during this interval, and any decrease in this delay might interfere with its operation. An increase in this delay could result in a lower maximum encoding rate.

Another interval which must be made small is the time required for the ramp to reach +10 volts and enter its useful region. This period is decreased by clamping the collector of Q_8 through D_5 to the voltage provided by the drop across D_6 and D_7. This causes the output voltage of the ramp generator to be clamped slightly above +10 volts, so the ramp enters

its useful region almost immediately after the turn-on delay. When the ramp reaches -0.2 volt Q_4 begins to conduct, producing a positive pulse which resets the ramp control multivibrator (Q_2 and Q_3). This causes Q_5 to conduct, shorting the summing junction to the -6 volt supply and resetting the ramp. The reset time is determined primarily by the open-loop bandwidth of the amplifier; therefore a lead network (R_{17} and C_9) is used for the prevention of oscillation. A compensation network which would provide a uniform slope of 20 db. per decade for the frequency response curve would also prevent oscillation but would result in a smaller open-loop bandwidth and hence a longer reset time.

The ramp is initiated by the sample-hold control multivibrator which triggers Q_2 into cutoff; Q_5 is cut off then, allowing the ramp to start. Emitter follower Q_1 provides the trigger signal for the reset pulse generator. When power is first applied to the encoder, it is possible for the ramp voltage to be negative and for the multivibrator to be in the wrong state (Q_3 conducting), in which case the circuit locks in this condition and does not

respond to trigger pulses. This situation is remedied by the initial set pulse, a negative step generated by the circuit described in the following section each time the encoder is turned on. The differentiated step cuts Q_3 and off and forces the circuit into the proper state.

3.8. Initial Set Pulse Circuit

An initial set pulse is required to set the ramp control multivibrator into the proper state when power is first applied to the encoder. Since the accompanying magnetic core memory unit requires a similar pulse, it was desired that the provision of the initial set pulses be automated rather than accomplished by a manual switch. A DPDT relay is used for convenience in choosing voltage levels, since the encoder and memory require different pulse voltages. The relay must be energized to produce these pulses only after all three power supply switches ($\pm$12 and -25 volts for the encoder and $\pm$6 volts for the memory) have been turned on. After a short delay ($\frac{1}{2}$ second) the relay must be de-energized to end the pulse and permit normal operation of the equipment.

These requirements are implemented in the circuit of Fig. 16. The relay coil is powered by the -25 volt supply, but no current can flow through it until the AND gate composed of Q_1 and Q_2 conducts. The relay is thus energized when the third power switch is turned on, regardless of the switching order. The voltage across the relay coil then causes current source Q_4 to conduct and to begin to charge C_1. After $\frac{1}{2}$ second the voltage across C_1 reaches 0.6 volt and Q_3 conducts. The current through D_3 cuts Q_2 off and the relay coil current drops to zero, ending the initial set pulses

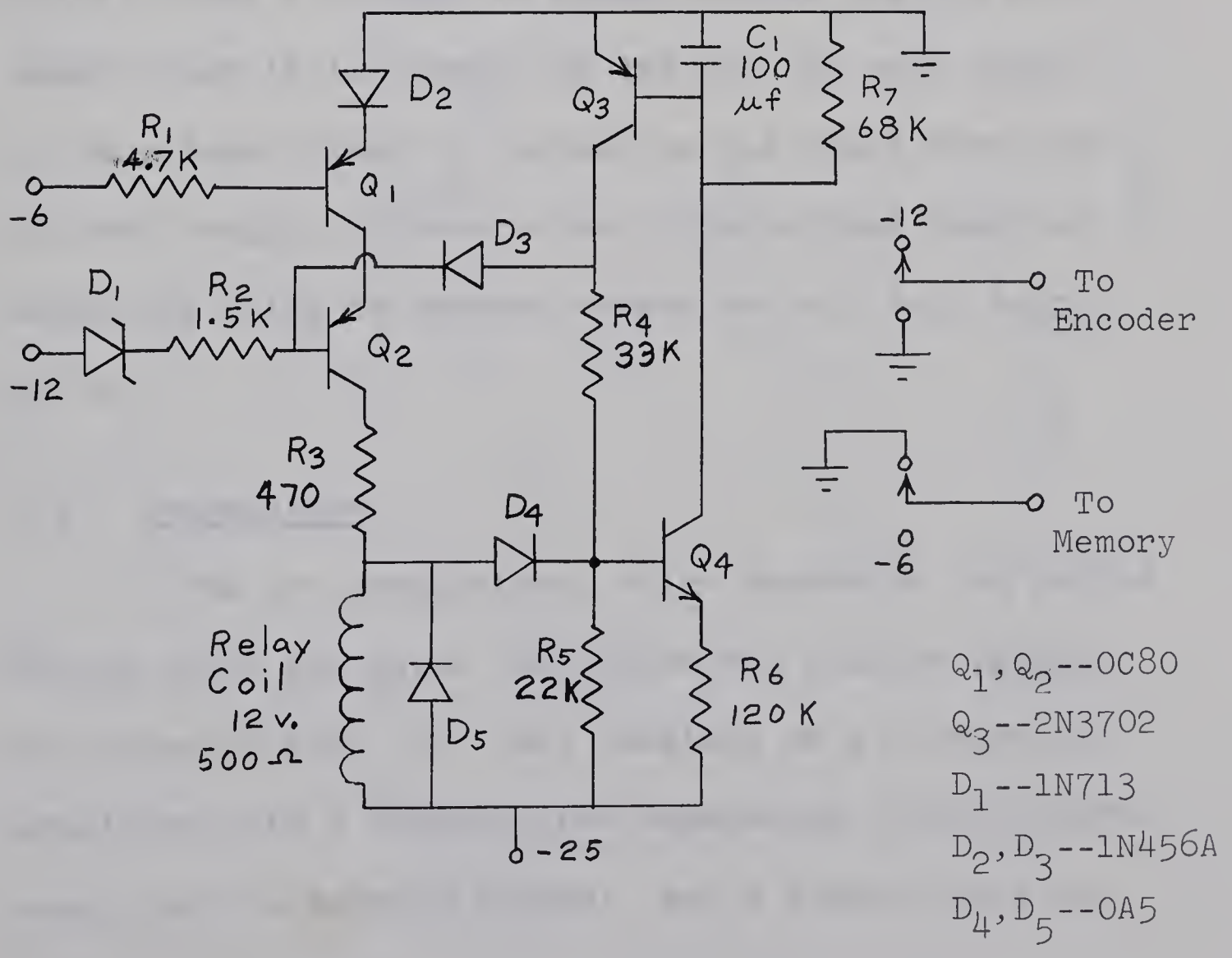
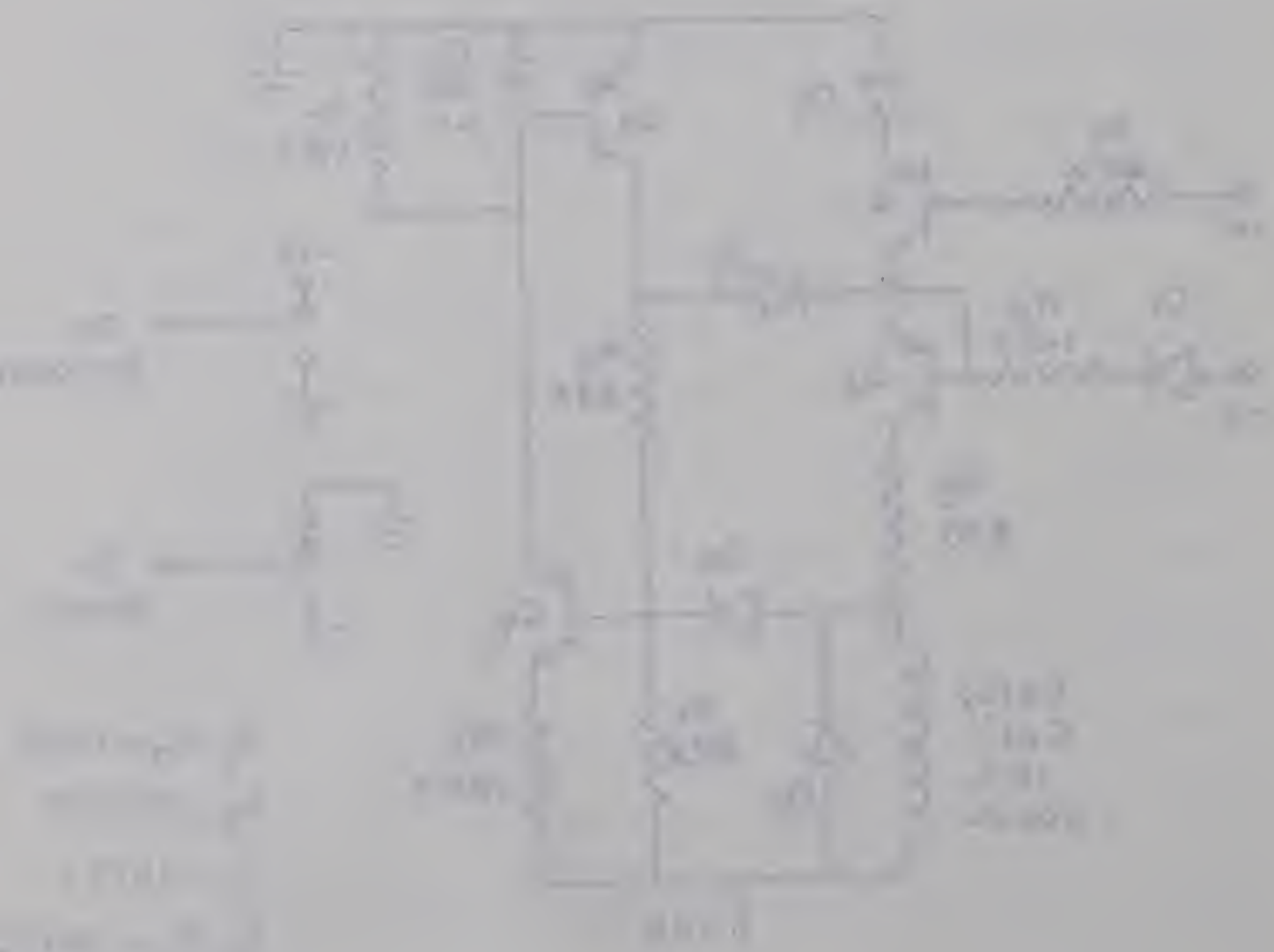


Figure 16. Initial Set Pulse Circuit

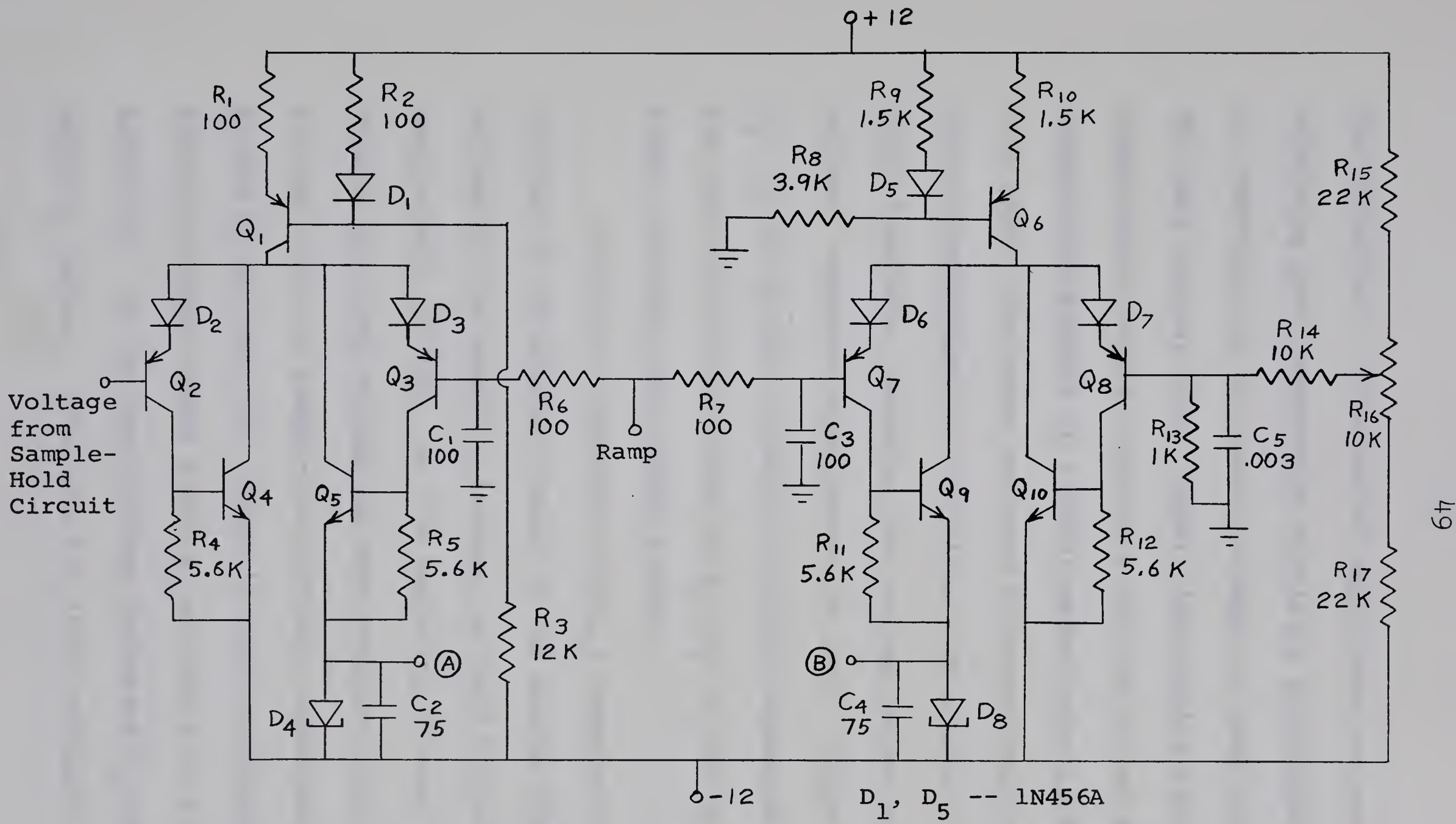


produced by the relay contacts. R_4 and R_5 now provide sufficient bias to keep Q_4 and hence Q_3 conducting, in order to prevent the relay from turning on again. Diode D_4 prevents the bias current through R_4 from being shunted through the low coil resistance. D_5 clips the voltage transient appearing across the relay coil when the current through it is stopped. R_7 discharges C_1 when the power supplies are turned off to prevent large variations in the length of the initial set pulses.

The clamped flip-flops used in the digital-to-analog converter (which is operated from the same supplies) cause a voltage to appear across the -12 volt supply when it is turned off and the -25 volt supply is on. Zener diode D_1 is used on the input from the -12 volt supply to ensure that this voltage does not allow the relay to operate unless the -12 volt supply is on.

3.9. Comparators

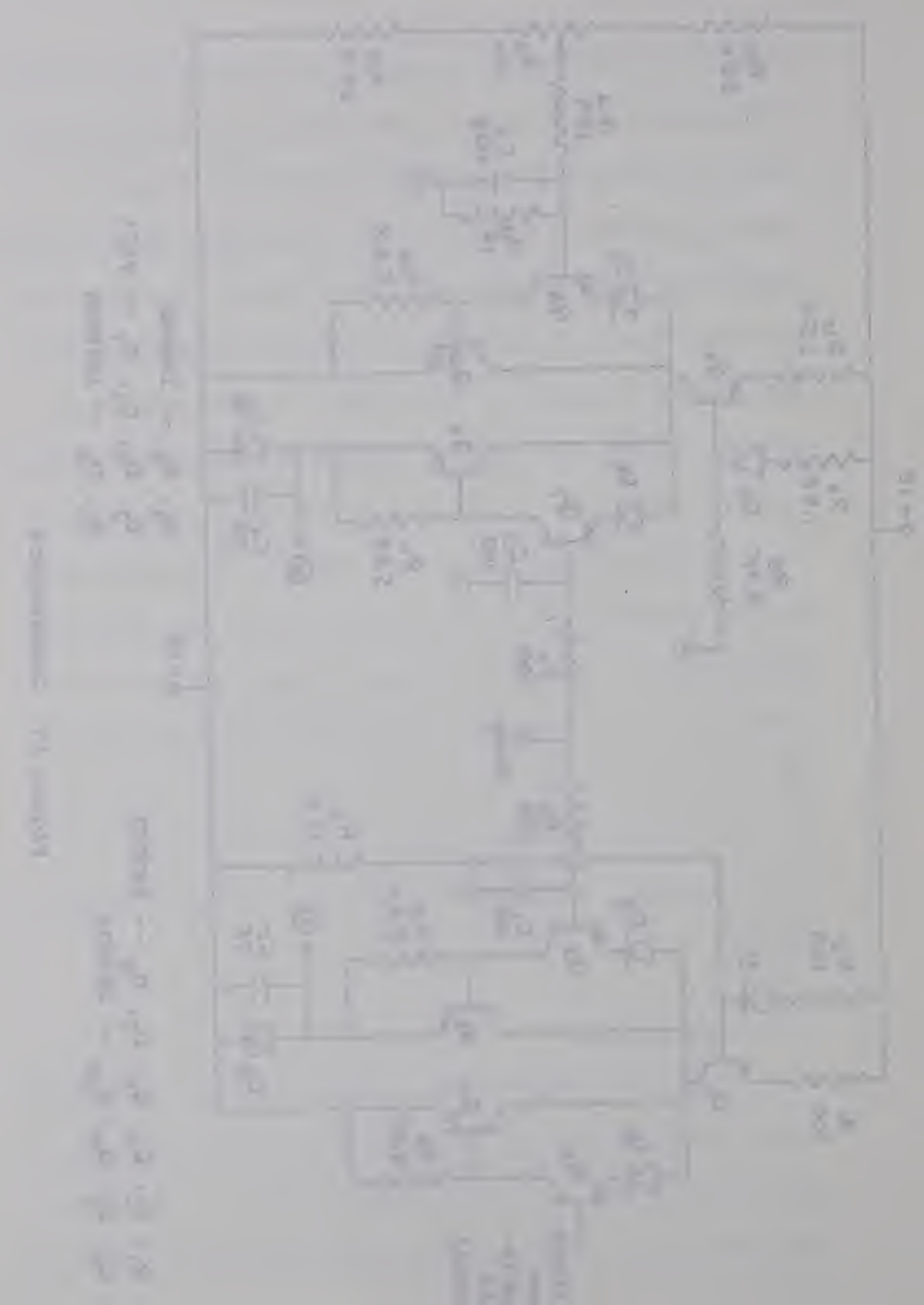
The two comparators, which determine the period during which the gated oscillator and counter operate, are shown in Fig. 17. Each consists of a differential amplifier with a temperature-compensated current source supplying the emitter current, and a tunnel diode in



Q_1, Q_2, Q_3, Q_6, Q_7, Q_8 -- 2N3702
Q_4, Q_5, Q_9, Q_{10} -- 2N3704

D_1, D_5 -- 1N456A
D_2, D_3, D_6, D_7 -- TI71
D_4, D_8 -- 1N2940A

Figure 17. Comparators



one collector. Differential amplifiers are used for obtaining good temperature stability and convenience in comparing the two input voltages to each comparator. The peak current of a tunnel diode varies little with temperature changes, and since the use of two similar comparators results in a first-order cancellation of this drift, the error produced by temperature changes in the comparators is negligible. To obtain a high input impedance, reducing the loading on the signal sources, compound transistors are used. Diodes D_2, D_3, D_6 and D_7 are included to prevent breakdown of the base-emitter junctions of Q_2, Q_3, Q_7 and Q_8 when these junctions are reverse biased.

The first comparator (Q_1-Q_5) compares the ramp voltage to the absolute value of the analog input voltage at the sampling instant, as held by the sample-hold circuit. At the beginning of each conversion the ramp voltage is more positive than the voltage from the sample-hold circuit; consequently Q_2 and Q_4 are cut off. There is then no current flowing through tunnel diode D_4 and hence no voltage across it. As the ramp voltage decreases Q_3 and Q_5 begin to conduct. When the two input voltages are

equal the currents in the two sides of the differential amplifier are equal. Current source Q_1 supplies a current of two milliamperes; when this is divided equally between the two sides of the differential amplifier, tunnel diode D_4 (having a peak current of one milliampere) switches to its high voltage state. The use of a current source rather than a resistor is necessary to maintain a constant current through the tunnel diode, independent of the sample-hold voltage, at the instant the two input voltages are equal.

The operation of the second comparator is similar, with the exception of the bias network on the base of Q_8. Instead of grounding this point, provision is made for a small adjustable voltage which cancels any difference in the comparators, such that when the analog input voltage is zero both comparators switch at precisely the same instant.

One difficulty encountered with this circuit is the interaction between the two comparators for analog input voltages very near zero. The interval between the switching of the two comparators should then be very short. At the instant the first comparator (D_4) switches, the current through D_8 is approaching its peak current, and even a small amount of energy at

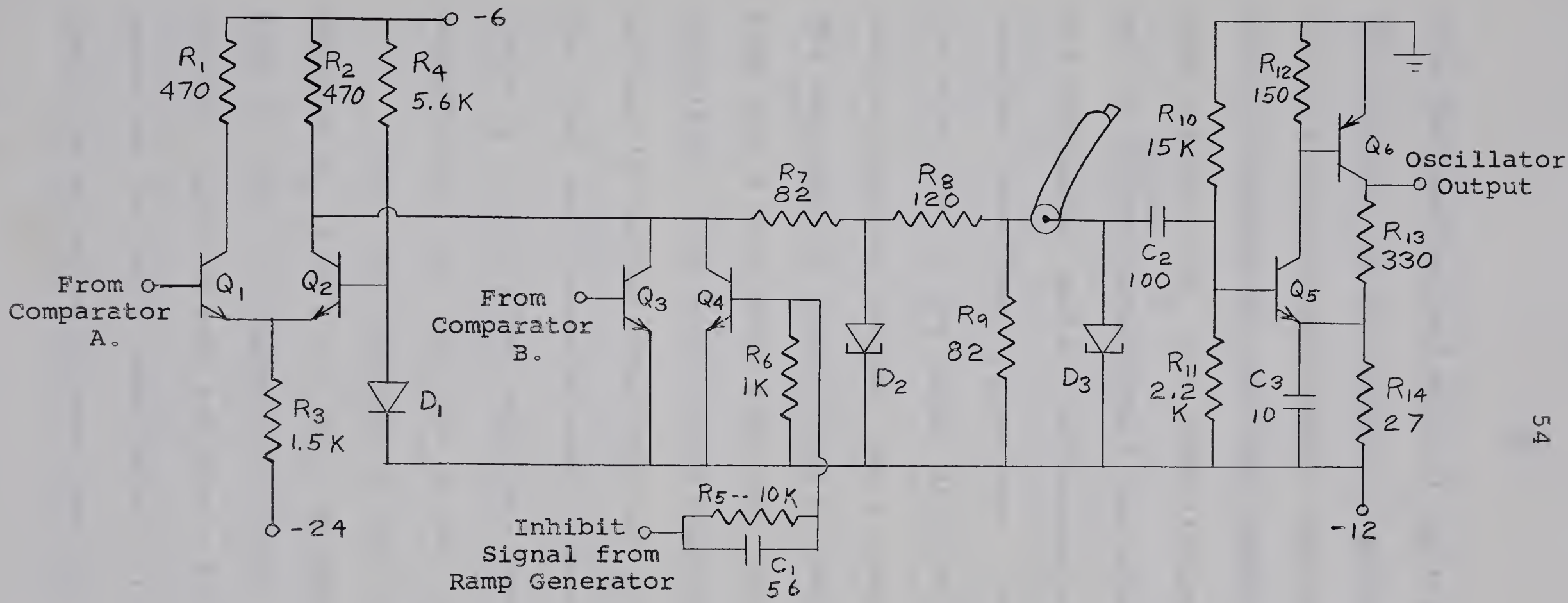
this time can cause the second comparator to switch prematurely. This energy can be in the form of radiation or power supply transients caused by the switching of D_8. Capacitors C_2 and C_4 reduce this effect, C_2 by increasing the switching time of D_4 and C_4 by increasing the energy required to switch D_8. The longer rise times then obtained are not harmful. In addition, the step from D_4 is fed back through the collector-to-base capacitance of Q_3 and tends to superimpose a transient on the ramp, again causing D_8 to switch at the same time as D_4. This effect is reduced by the use of low-pass filters (R_6, C_1, R_7 and C_3); it cannot be entirely eliminated, however. This source of error is discussed further in Section 4.2.

3.10. Gated Oscillator

The gated oscillator (Fig. 18) is actuated by signals from the two comparators described in the previous section. The gating is done by the first four transistors which act as current switches. At the beginning of a conversion Q_1, Q_3 and Q_4 are cut off, while Q_2 conducts most of the current from R_2. Little current then flows through D_2, maintaining it in its low voltage state. When the ramp voltage is

equal to the voltage from the sample-hold circuit, the input voltage from comparator A switches from -12 to -11.5 volts, causing Q_1 to conduct and Q_2 to cut off. Current through R_2 can then pass through R_7 to D_2, which switches to its high-voltage state. When the ramp crosses zero volts the tunnel diode in comparator B switches to its high-voltage state, saturating Q_3. The current through R_7 then decreases to practically zero, and D_2 returns to its low-voltage state. Immediately the ramp resets, automatically resetting the comparators in the order which would allow D_2 to return to its high voltage state for a short time, unless prevented. Q_4 is switched on by the inhibit signal from the ramp control multivibrator while the ramp is being reset, maintaining D_2 in its low-voltage state during this period. Thus D_2 is in its high-voltage state only during the interval between the two comparator pulses, the period during which the oscillator should operate. The voltage across D_2 can then be used to control the oscillator.

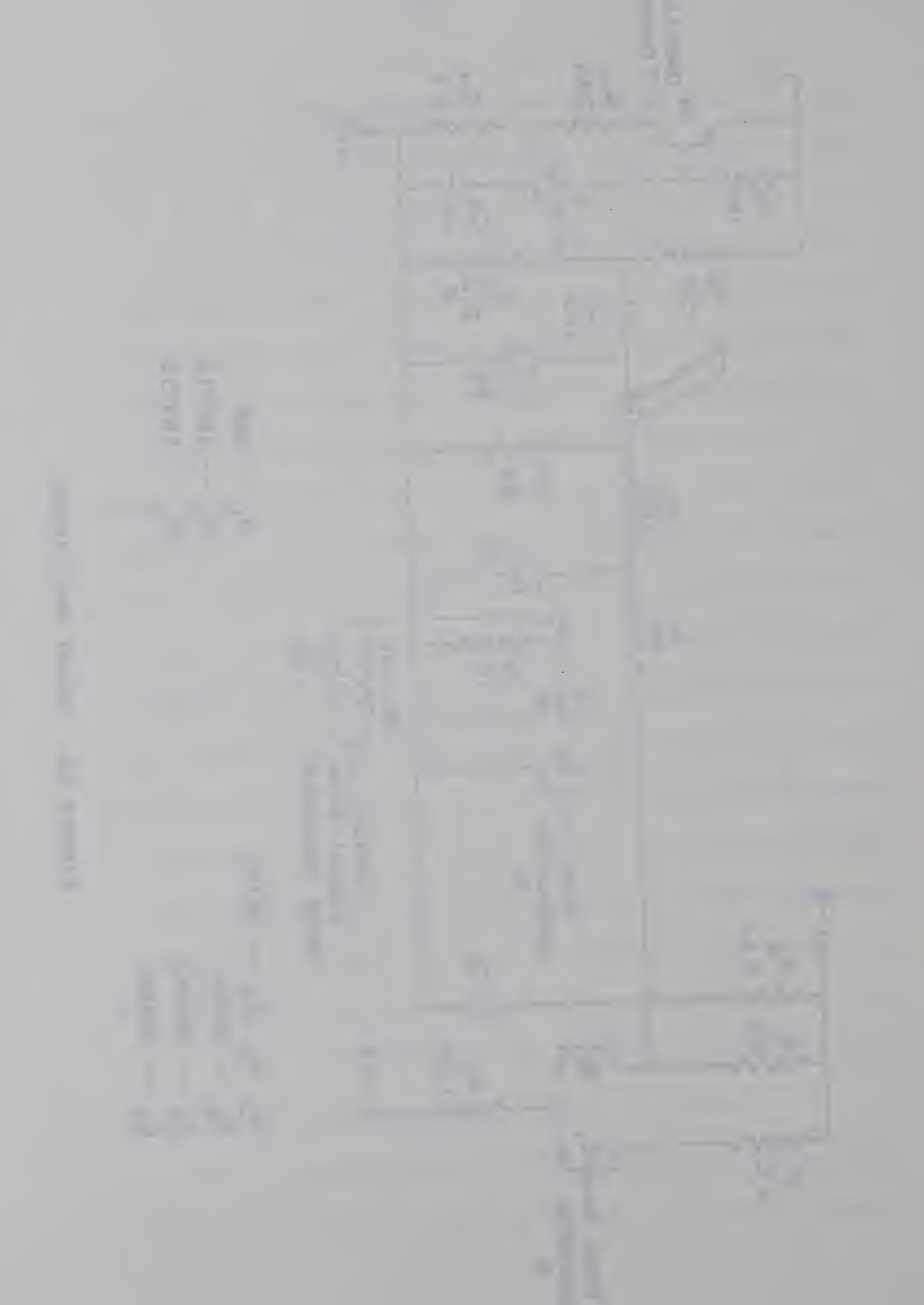
D_2 acts as a power supply for the tunnel diode oscillator D_3, with R_8 and R_9 being chosen to bias D_3 in its negative resistance region (a necessary condi-



Q_1, Q_2, Q_3 -- 2N797
Q_4 -- 2N706
Q_5 -- 2N3563
Q_6 -- 2N3640

D_1 -- OA5
D_2 -- 1N3716
D_3 -- 1N3712

Figure 18. Gated Oscillator



tion for oscillation) while D_2 is its high-voltage state. The frequency of oscillation is governed by the length of the shorted coaxial cable. Oscillation can take place at any frequency at which the shorted line appears as an open circuit to D_3 (i.e. when its length is an odd number of quarter wavelengths), and since this includes the fundamental and all odd harmonics the oscillator waveform resembles a square wave. Because of the finite rise time of the tunnel diode voltage, the cable used is slightly shorter than a quarter wavelength. The switching of tunnel diode D_2 provides a voltage step with a very short rise time for starting the oscillator. The steady-state amplitude of the oscillations is reached after only two cycles, and even the first negative-going edge produced by the oscillator is of sufficient amplitude (when amplified) to trigger the first flip-flop in the counter.

Since the amplitude of the oscillations produced by D_3 is only 0.4 volt, an amplifier is necessary in order to trigger the counter. Q_5 and Q_6 provide a gain of ten, and have a high input resistance and low input capacitance to provide good isolation of the oscillator from its load. Capaci-

tor C_3 increases the amplifier gain at very high frequencies, resulting in rise and fall times of less than four nanoseconds. These are adequate for triggering the counter at rates in excess of 60 megahertz.

3.11 Counter

The binary counter consists of ten flip-flops connected such that the negative-going edge of the trigger output of each flip-flop triggers the next. Each flip-flop operates at half the switching rate of the previous one, and because of the great range of trigger pulse rates (500:1) between the fastest and the slowest flip-flops, three different circuits are used.

A standard saturated bistable multivibrator is shown in Fig. 19; it is used for each of the six flip-flops which operate at trigger rates of 4 mhz. or less. The bit output and the trigger signal for the following flip-flop are taken from opposite sides of the flip-flop. An emitter follower (Q_3) is necessary to isolate the output wiring capacitance from the collector of Q_2. R_8 and D_2 make provision for resetting the flip-flop before each conversion.

Three flip-flops of the type shown in Fig. 20

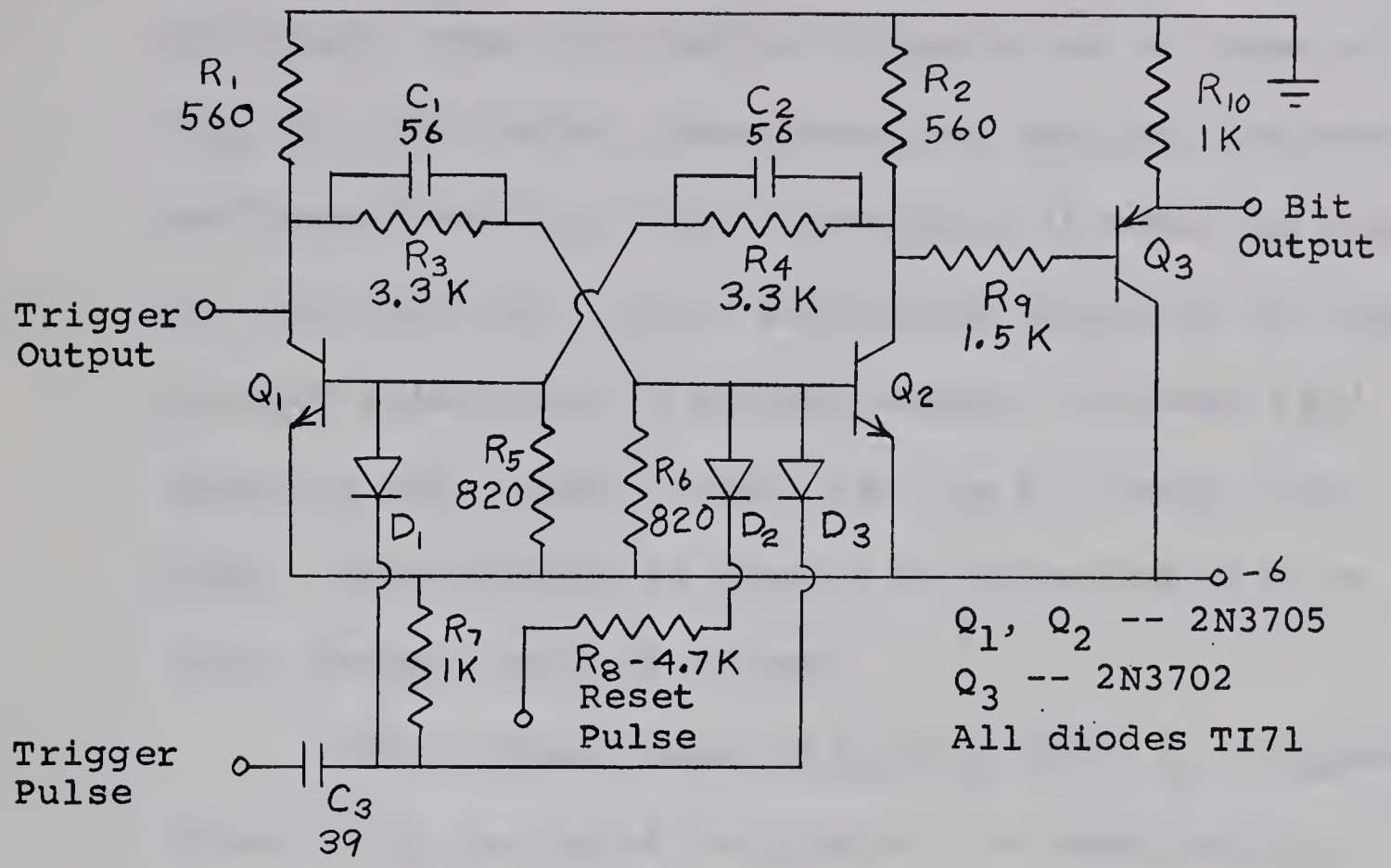


Figure 19. Low Speed Flip-Flop

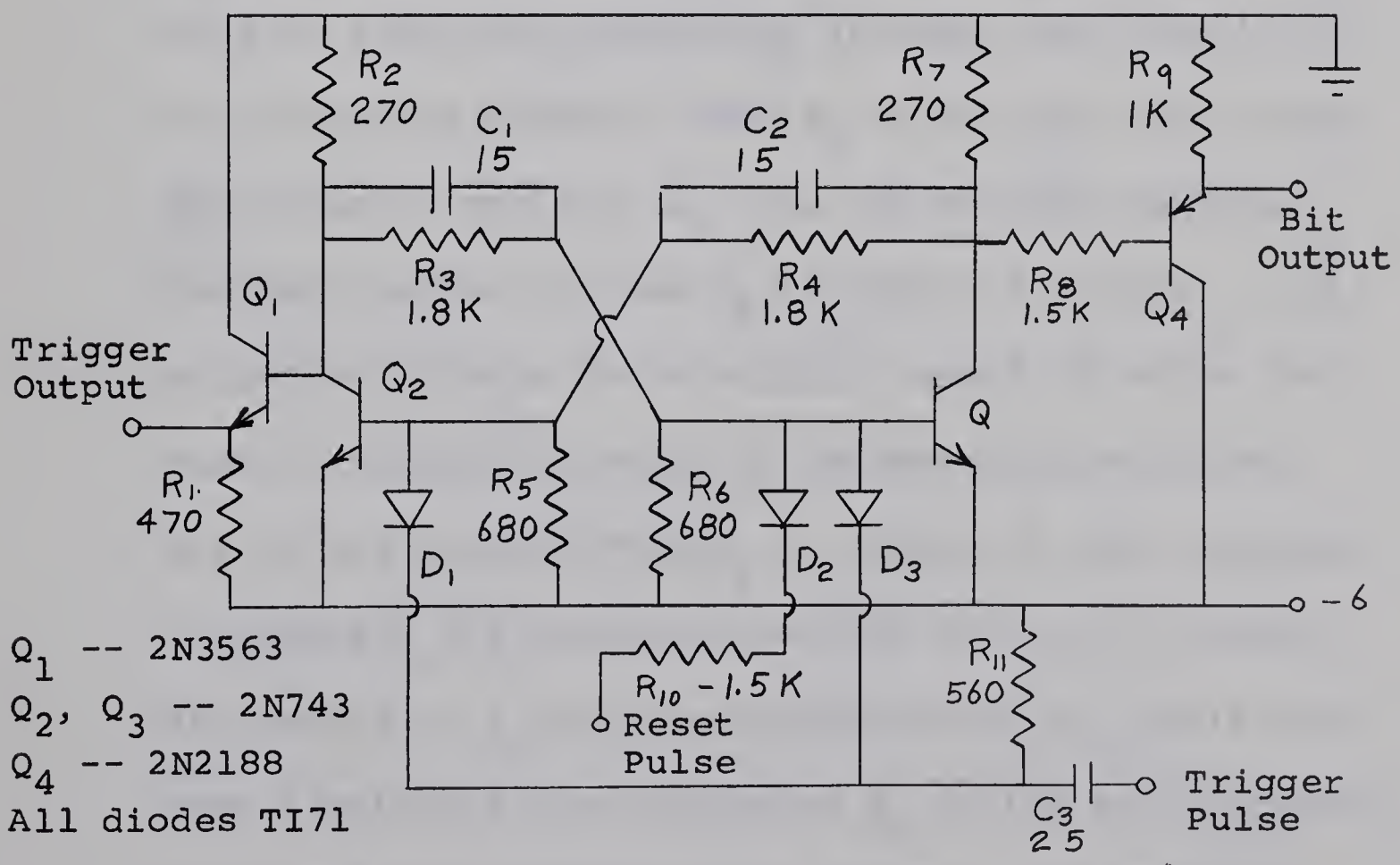
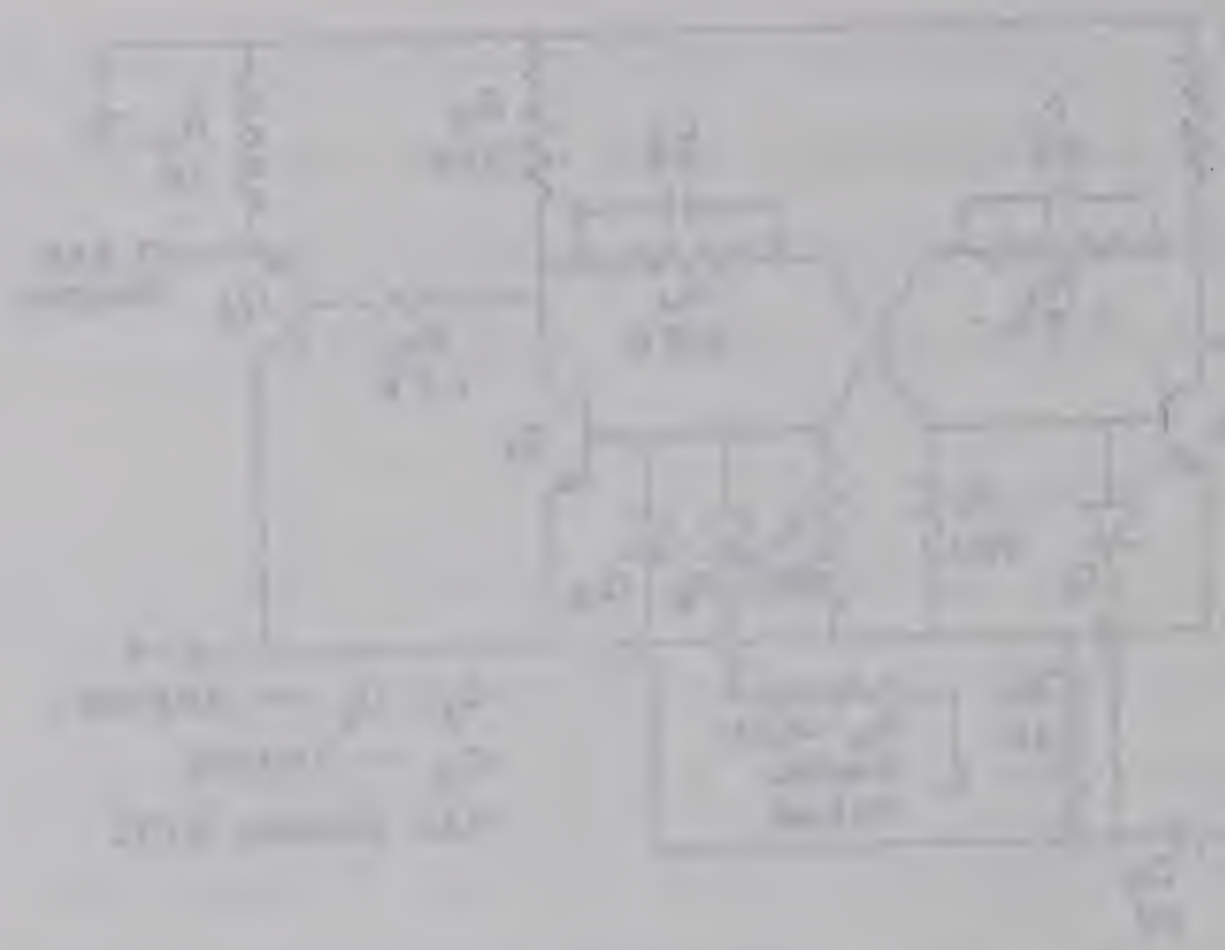
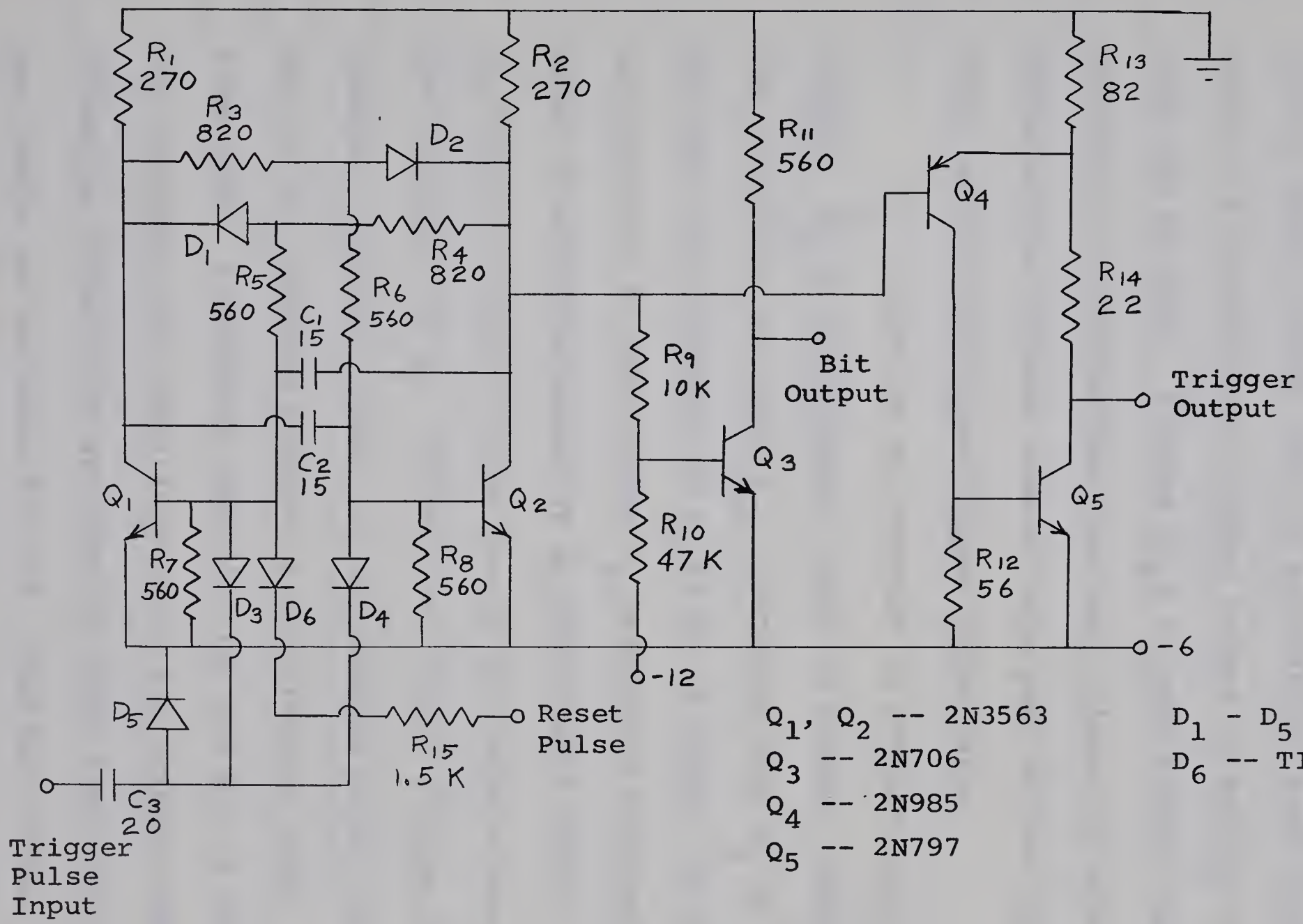


Figure 20. Medium Speed Flip-Flop



are used. They are similar in operation to those of Fig. 19, but faster transistors and smaller resistances and capacitances are used throughout in order to reduce the rise and fall times, permitting operation at higher trigger pulse rates. Another emitter follower (Q_1) supplies the trigger signal for the following flip-flop. This circuit is capable of operating with an input trigger rate of 32 mhz.

The highest speed flip-flop, which is triggered directly by the gated oscillator, is shown in Fig. 21. It is a non-saturated flip-flop in which D_1 and D_2 are used to prevent saturation of Q_1 and Q_2 (and thus to avoid the consequent storage time delay) in the following manner: When Q_2 is cut off and a trigger pulse is applied, Q_1 cuts off and the positive feedback present causes Q_2 to begin to conduct. Its collector voltage drops rapidly toward -6 volts, but when it reaches -5 volts D_2 becomes forward-biased. Any of the current from R_3 in excess of that required to maintain the collector voltage of Q_2 at -5 volts, is shunted by D_2 into the collector of Q_2. This current limiting action maintains Q_2 in the active region until the next trigger pulse occurs. The negative-



Q_1, Q_2 -- 2N3563
Q_3 -- 2N706
Q_4 -- 2N985
Q_5 -- 2N797

D_1 - D_5 -- 1N3604
D_6 -- TI71

Figure 21. High Speed Flip-Flop

going trigger pulses, produced by D_5 and C_3 when they differentiate the input square wave, cause the conducting transistor to cut off; if this transistor is in the active region rather than in saturation, less trigger energy is required and trigger pulses of smaller amplitude can be used. A diode (D_5) is used rather than a resistor to differentiate the input signal in order to decrease the recovery time of this part of the flip-flop, permitting higher trigger pulse rates.

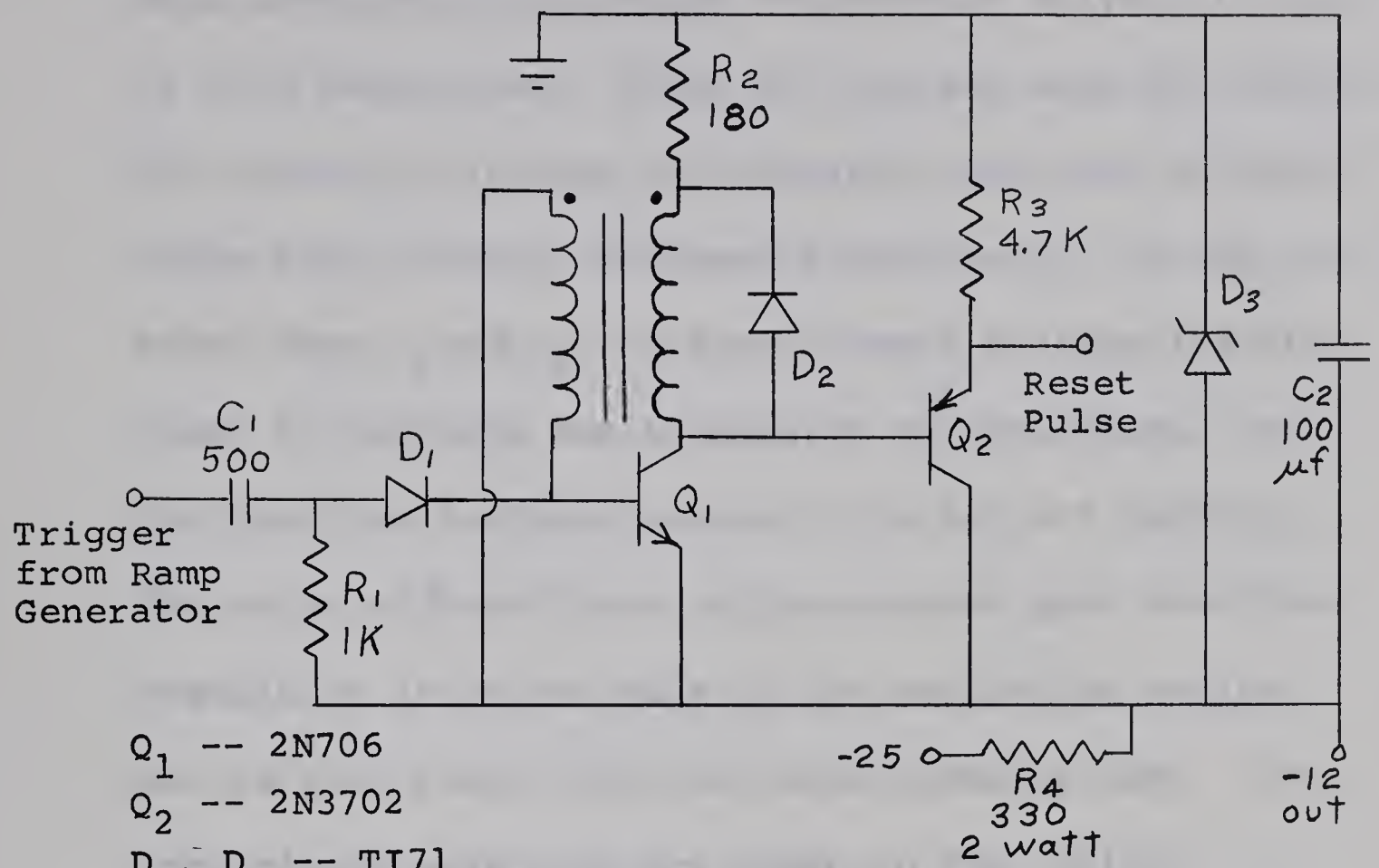
Q_3 is used as an inverter to provide the bit output. R_9 is sufficiently large to prevent loading of the flip-flop, and with R_{10} it ensures that Q_3 is cut off when the collector of Q_2 is at -5 volts. No speed-up capacitor is used across R_9 because of the degradation of switching speed of Q_2 which would result. Q_3 therefore cannot follow the 32 mhz. square wave at the collector of Q_2. The correct output voltage is reached, however, within 0.3 microsecond after the end of the encoding process, a satisfactory short rise time. A feedback amplifier (Q_4 and Q_5) is used for isolation and amplification of the trigger signal. Germanium transistors are used in order that the voltage levels are suitable for D.C. coupling without

saturating or cutting off Q_4 or Q_5. A.C. coupling is not desirable here because the first change of state of the flip-flop produces a pulse of larger amplitude than the following pulses. This larger first pulse would drive an A.C. coupled amplifier into saturation (since the output amplitude is almost equal to the supply voltage) and the following few pulses would be clipped. Q_4 and Q_5 are operated at relatively large currents to obtain a large gain-bandwidth product.

3.12. Reset Pulse Generator

The reset pulse generator (Fig. 22(a)) is a monostable blocking oscillator which is triggered by the same pulse that initiates the ramp, and which resets all the flip-flops in the counter during the initial turn-on delay of the ramp. Q_1 provides a rectangular pulse with rise and fall times of 20 nanoseconds and a duration of 0.35 microsecond, long enough to reliably reset the counter but sufficiently short that it does not interfere with the encoding process.

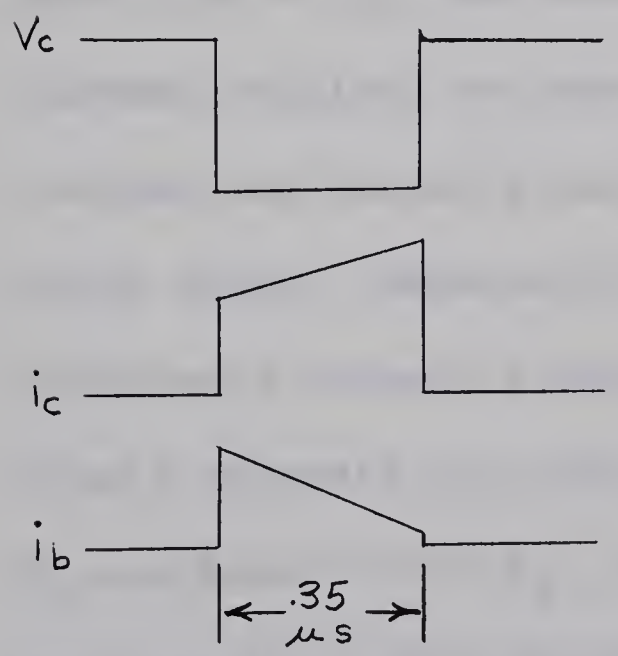
Q_1 is normally cut off; when a trigger pulse occurs Q_1 begins to conduct, and the positive feed-



Q_1 -- 2N706
Q_2 -- 2N3702
D_1, D_2 -- TI71
D_3 -- 1N759A

Transformer 2:1, 50 μh.

22(a) Circuit



22(b) Waveforms

Figure 22. Reset Pulse Generator

back provided by the pulse transformer drives it rapidly into saturation. After its initial step the collector current continues to increase, while the initially large base current decreases toward zero. At the instant when $i_c = \beta i_b$ the base current becomes insufficient to maintain the transistor in saturation, and the positive feedback causes it to cut off rapidly. The value of β used here is the current gain when the transistor is on the edge of the saturation region, and is much lower than the value normally used. The approximate waveforms are shown in Fig. 22(b).

Diode D_2 limits the large voltage transient which would occur across the pulse transformer at the end of the pulse, thereby preventing the destruction of Q_1. Emitter follower Q_2 provides the current required to reset the counter without loading the blocking oscillator and affecting its pulse width. Because of the large power supply transients caused by this circuit, it is operated from a separate -12 volt course provided by R_4, C_2 and Zener diode D_3. This also supplies the sample-hold control multivibrator, the only other switching circuit requiring a -12 volt supply.

3.13. Voltage Regulators

In addition to the available power supplies, a -6 volt source is required for the operation of the counter (to produce the correct ouput logic levels) and for several other switching and analog circuits. In order to keep the analog circuit supply voltage free from switching transients, two separate voltage regulators are used. One is designed to supply 200 ma. for the switching circuits, while the other supplies approximately 40 ma. for the analog circuitry.

Both the voltage regulators of Fig. 23 and 24 utilize negative feedback to obtain a lower output impedance, in order that the change in output voltage is small when the load current varies. These regulators differ from the usual power supply circuits in that since the power source is the well-regulated -12 volt supply, there is no power line frequency ripple to be removed; only the small high-frequency switching transients need be eliminated. Also, there is no need for a Zener diode to provide a voltage reference for the regulator; a voltage divider (R_1 and R_2) performs the same function, with C_1 to filter out high frequency transients. The differential amplifier in each regu-

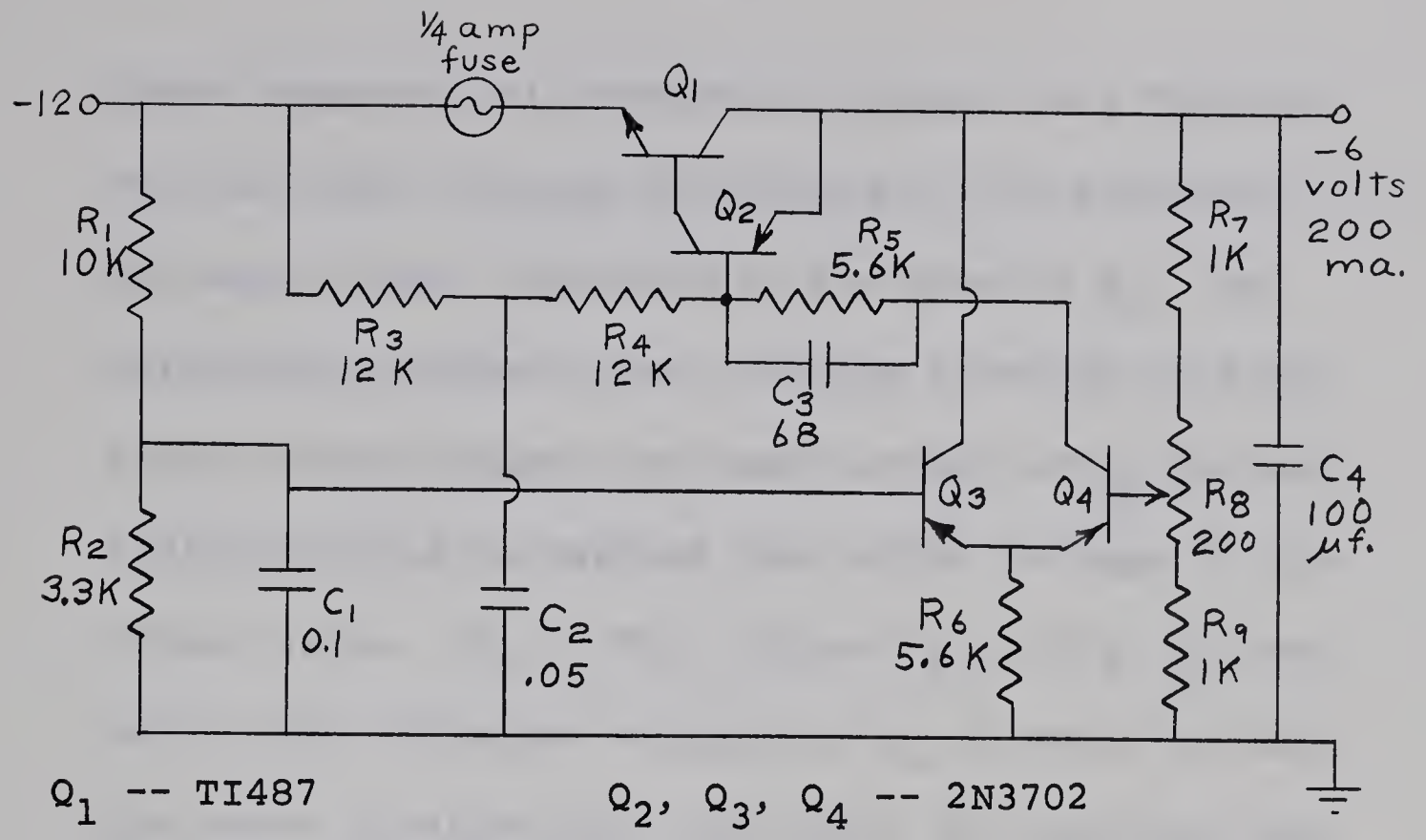


Figure 23. Switching Circuit Regulator

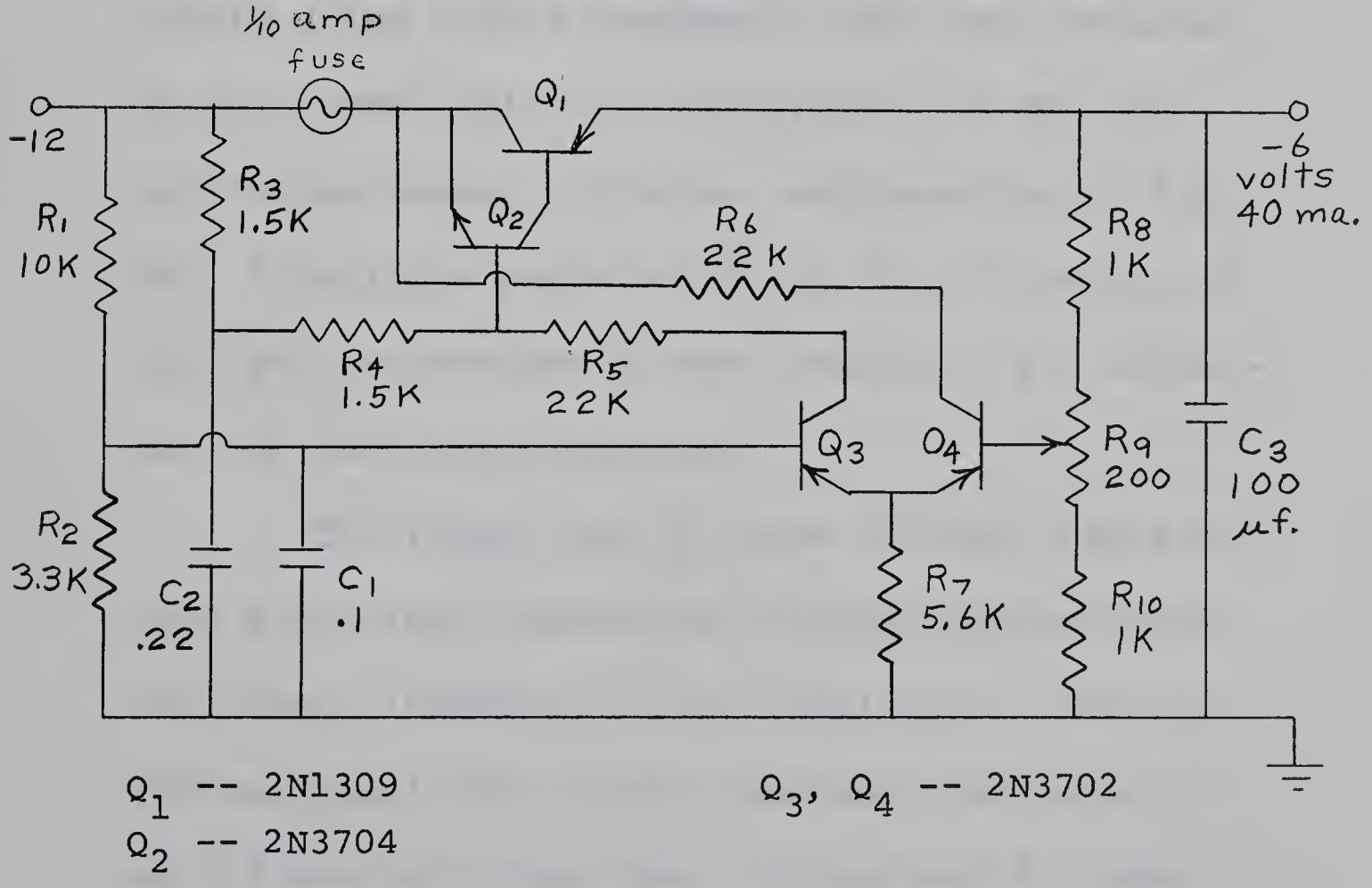
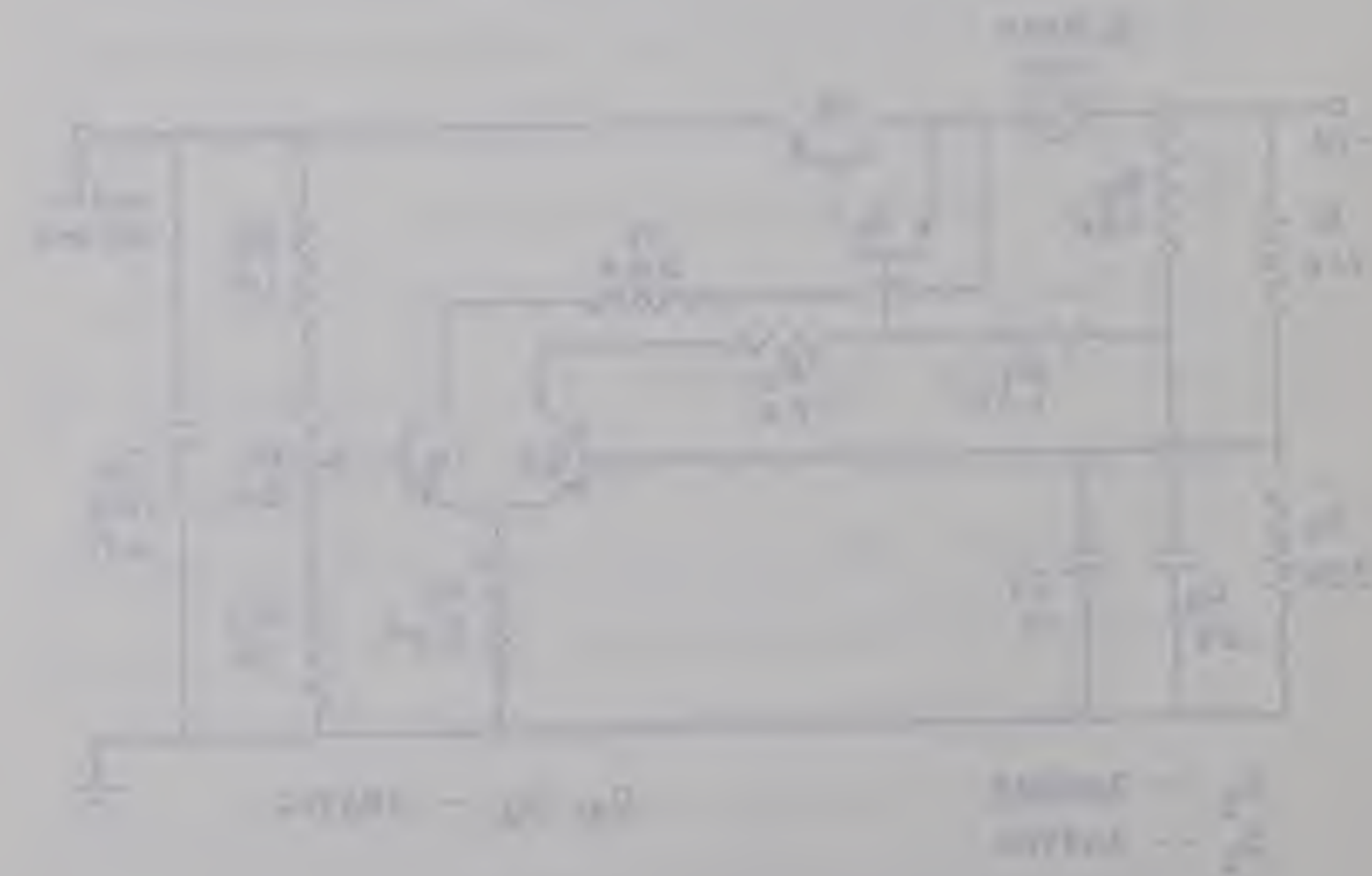


Figure 24. Analog Circuit Regulator



lator compares this reference voltage to a fraction of the output voltage determined by the resistive voltage divider connected to the base of Q_4. Any difference between these voltages provides an error signal which changes the base current of Q_2 in such a direction as to restore the output voltage to its proper value. R_5 in Fig. 23 and R_6 in Fig. 24 each reduce the collector voltage of Q_4 in order to make the power dissipations, and hence the junction temperatures, of Q_3 and Q_4 equal. Two-transistor compounds (Q_1 and Q_2) are used in each regulator to obtain a low output impedance; they are connected in the common emitter configuration in Fig. 23, and in the common collector configuration in Fig. 24. A variable resistor (R_8 in Fig. 23 and R_9 in Fig. 24) is provided in each regulator for adjustment of the output voltage.

The fuses used in these voltage regulators have sufficient resistance to affect appreciably the output impedance of the regulators. For the 200 ma. supply the output impedance was measured as 0.8 ohms with the fuse in place and 0.2 ohms with the fuse shorted. Similarly, for the 40 ma.

supply the output impedance was 0.30 ohms with the fuse and 0.13 ohms without the fuse. The operation of the regulators is satisfactory, however, with the larger output impedances, and the fuses protect Q_1 in each circuit in the event that the output is accidentally shorted.

CHAPTER 4

RESULTS AND CONCLUSIONS

4.1. Construction

The encoder was assembled on thirteen 4 x 6" epoxy-fiberglass printed circuit boards and mounted on a standard 19½" rack, using plug-in printed circuit board connectors. Among the parts used in the encoder were 126 transistors, 86 diodes, 344 resistors and 120 capacitors.

A great deal of difficulty was encountered in the reduction of switching transients which would cause serious errors in the encoder. Separate power supply and ground wires were used for most of the circuits to reduce ground loops. Metal shields were installed between some of the printed circuit boards to shield the summing junctions of the operational amplifiers from the switching transients produced by other circuits. In addition, low-pass filters of the type shown in Fig. 25 were included on most of the printed circuit boards. These are similar in every case and are not shown on all the circuit diagrams.

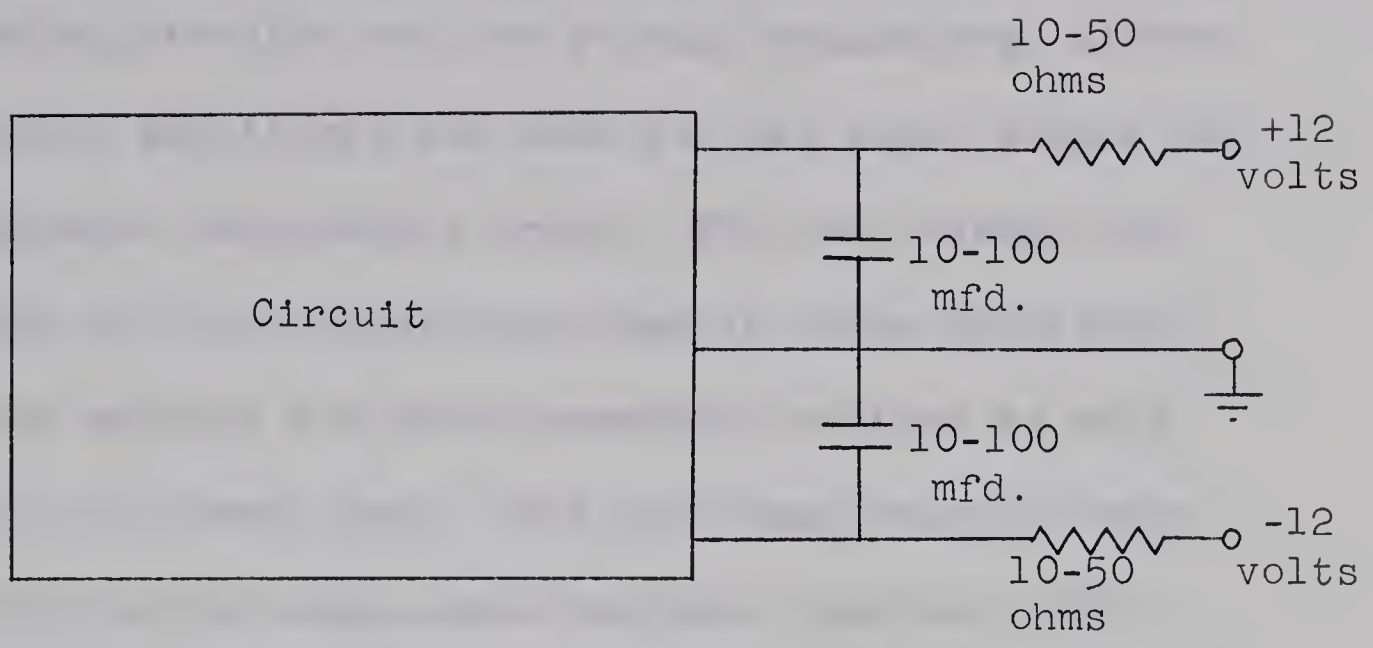


Figure 25. Power Supply Filtering

4.2. Encoder Accuracy

In specifying the accuracy of an analog-to-digital converter, several sources of error must be considered individually. The most obvious of these is the nonlinearity of the ramp; any curvature in excess of that calculated in Section 3.7 would cause deterioration of the encoder accuracy. This was investigated by encoding known D. C. voltages throughout the range of the encoder and comparing the encoded outputs with the binary coded equivalents of the input voltages. No error was detected, indicating that the ramp linearity is well within the required 0.1%.

Another possible source of error is drift due to changes in ambient temperature. In all the

analog circuits and the voltage regulators, differential amplifiers are used for the input stages to decrease temperature drift. The low leakage current silicon transistors used in these amplifiers were matched for base-to-emitter voltage as well as for current gain. The two transistors in each differential stage were fastened together with epoxy cement and insulated to minimize the temperature difference between them.

The variation of oscillator frequency is another undesirable effect of ambient temperature changes. This drift was measured as +150 ppm/^{o}C. Fortunately, the effect of this drift can be reduced by introducing an opposing drift in the slope of the ramp. By using a wirewound input resistor with a temperature coefficient of +20 ppm/^{o}C. and a polystyrene feedback capacitor with a coefficient of -120 ppm/^{o}C. in the ramp generator, the resulting temperature coefficient is +50 ppm/^{o}C., small enough to cause negligible error in the specified temperature range. The overall effect of temperature changes could not be measured because an oven sufficiently large to

accommodate the entire encoder was not available.

The interaction between the two comparators, described in Section 3.9, is a further source of error for small input voltages. This error was evaluated by slowly increasing the input voltage from zero and measuring the voltages at which switching between adjacent output states occurred. This is necessarily an approximate measurement since, due to the effects of noise, the output switches between adjacent states over a range of input voltage of approximately four millivolts. However, the switching point was considered to be the voltage level for which the output was in each of the adjacent states for half of the time, as judged from the relative intensity of the two oscilloscope traces. The resulting idealized graph of Fig. 26 shows that the amplitude of the dead zone is 17 millivolts and that the encoded output is correct for input voltages greater than 70 millivolts. For this reason the encoder is calibrated at 80 millivolts and 10 volts, rather than at zero and 10 volts. The error contributed by this dead zone is not considered ser-

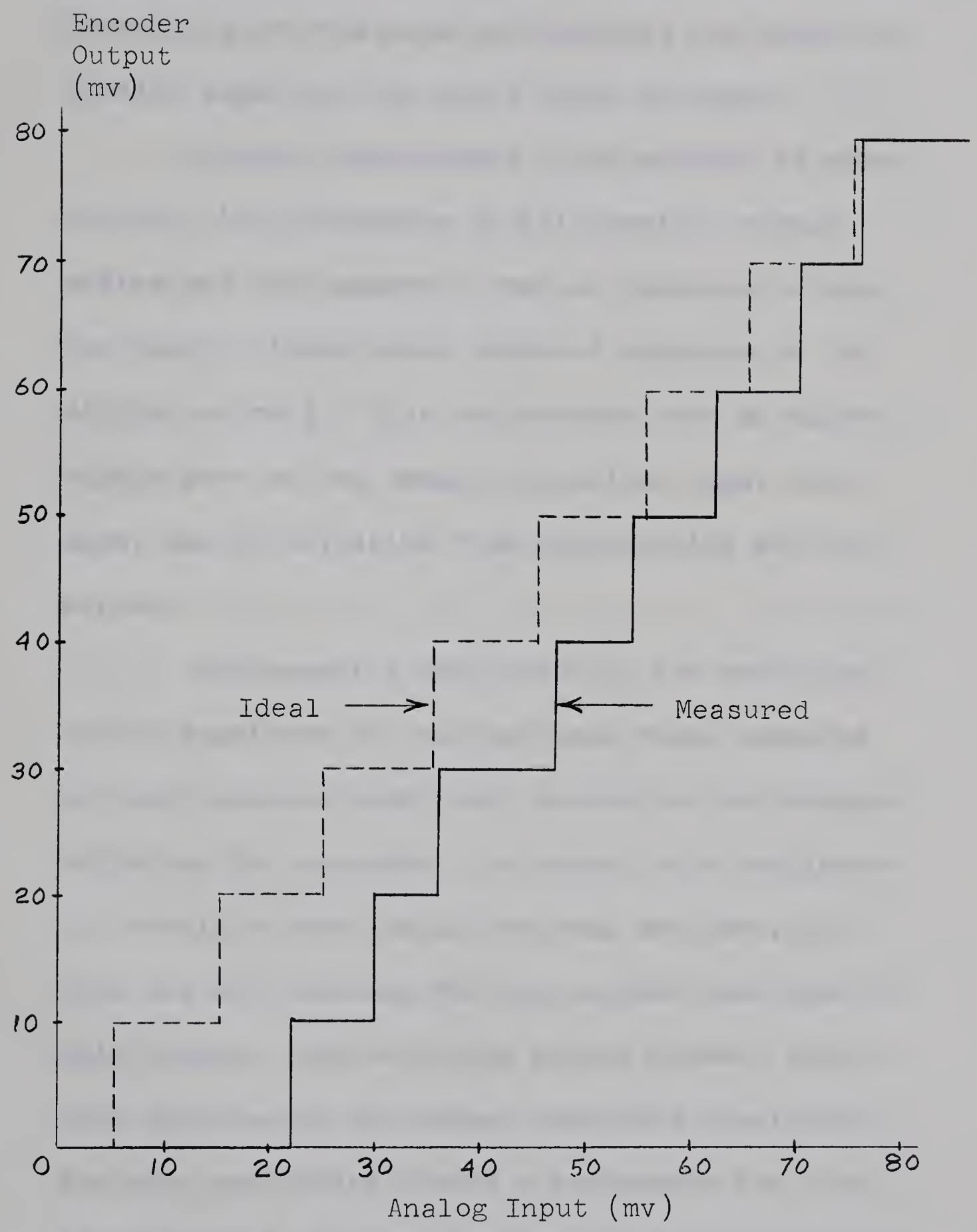


Figure 26. Encoder Dead Zone

ious, however, since the encoder is to be used with an analog computer. Other analog computing equipment (notably quarter-square multipliers) has errors of similar magnitude for small input voltages.

Another requirement of an encoder is monotonicity (the existence of all possible output states and the assurance that an increase in analog input voltage never causes a decrease in the digital output). This was checked over an appreciable part of the range of possible input voltages, and no deviation from monotonicity was observed.

Differential nonlinearity, the variation of the magnitude of the quantized steps compared to their average magnitude, is another performance criterion for encoders. In theory this nonlinearity should be very small for ramp encoders, but this was not the case for the encoder described in this thesis. The switching points between states were measured in the manner described previously; the step amplitudes showed a preference for 7 and 13 millivolts, and the extreme sizes observed were 3 and 18 millivolts. The percentage nonlinearity

decreases by approximately a factor or two for each more significant bit, so to some extent resolution and differential nonlinearity can be traded by neglecting some of the least significant bits. This nonlinearity is partially a result of the oscillator waveform. The negative-going edge produced when the oscillator is stopped should be of sufficient amplitude to trigger the counter during precisely half of the oscillator cycle. Since this is not the case, the preferred step amplitudes are slightly different from 10 millivolts. Switching transients from the oscillator and counter which become superimposed on the ramp, and transients from the counter which tend to modulate the oscillator output amplitude, also contribute to the differential nonlinearity. These effects were reduced by the use of separate power supply and ground wires for the circuits involved and by filtering, but could not be eliminated entirely.

In addition to the above sources of static error, there are two other possible sources of error which can become significant for rapidly changing analog input voltages. The first of these

is the switching delay of the absolute value circuit, discussed in Section 3.4, which results in a temporary negative output voltage from the absolute value circuit immediately after a change in the polarity of the analog input voltage. The remainder of the encoder interprets this negative voltage as zero volts, so the magnitude of the error is a linear function of the rate of change of the analog input voltage. This delay was measured as 0.2 microsecond, so the maximum error produced (for the worst-case rate of change calculated in Section 3.1) is less than 0.2 volt. The error is proportionally less for smaller rates of change and only occurs occasionally, whenever the sample-hold circuit begins to hold within 0.2 microsecond of the zero crossing instant.

The other possible source of dynamic error is the charging of the holding capacitor in the sample-hold circuit through a large change in voltage at the beginning of the encoding process. An insufficiently well-behaved transient response of the sample-hold circuit could cause an overshoot or ringing during the sampling interval,

producing an error roughly proportional to the change in voltage between samples. This effect was investigated using single pulses to trigger the encoder and changing the input voltage over the full range of the encoder between samples; no such error was observed.

4.3. Conclusions

The objective of constructing an analog-to-digital converter satisfying the requirements stated in Section 1.2 has been achieved. However, as better components become more readily available at decreasing prices, some improvements could be made in the future.

Integrated circuits could be used to replace many of the circuits in the encoder, resulting in a considerable decrease in physical size. MOSFETs could be used instead of the series switching transistors in the absolute value circuit. This would result in smaller switching transients following changes in the polarity of the analog input voltage (perhaps sufficiently small that the unity gain amplifiers preceding these switches could be

omitted).

If the frequency of the oscillator and the switching rates of the flip-flops in the counter could be doubled, the absolute value circuit could be eliminated entirely, as discussed in Section 2.2. This would effect a considerable reduction in the cost and complexity of the encoder.

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